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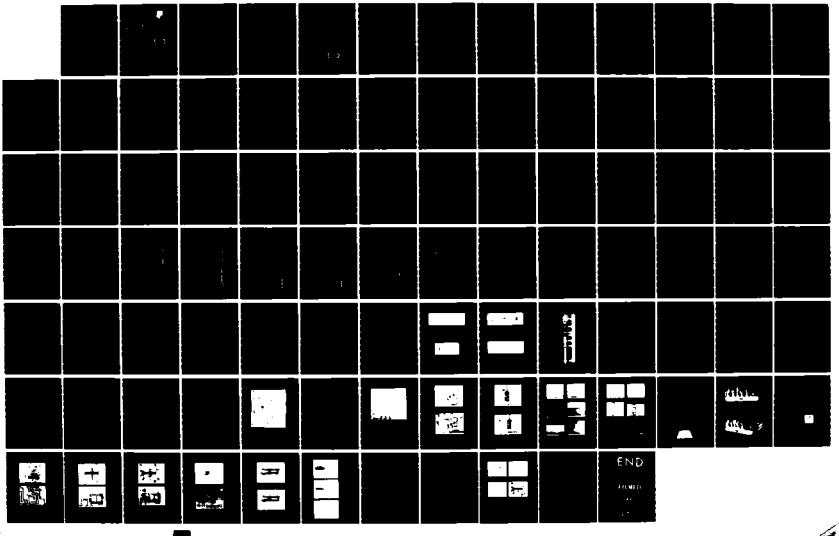

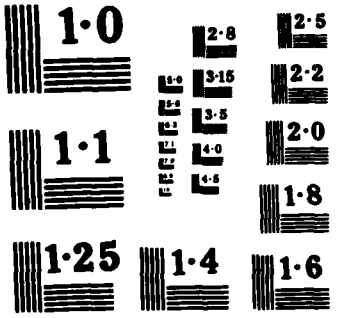

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INVESTIGATION OF MARGINAL VOLTAGE ANALYSIS FOR DEFECT LOCATION IN INTEGRATED CIRCUITS

ERA Technology Ltd.

E. F. Maher

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Digital integrated circuits tend to be classified as either good or bad when tested by standard equipment. Standard testing techniques fail to detect a group of circuits that pass normal testing but then fail after a short time of actual use. These circuits represent a reliability hazard for systems. For high reliability applications a "burn-in" test is used to eliminate these devices with latent defects. Some devices though survive the "burn-in" test only to fail later for reasons usually associated with failure mechanisms that are not accelerated by the "burn-in" test. An alternate screening technique is needed to eliminate these devices. A technique for detecting these reliability rogues has been studied along with a modification to the technique that will allow a more rapid location of the physical defect sites.

The objective of this effort was to investigate a new technique for locating faults in complex integrated circuits. The technique combines a global device electrical test called

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marginal voltage analysis with local area stimulation (E-beam or optical source) of the device surface to locate fault sites. In marginal voltage analysis the supply voltage is lowered until the circuit just fails to operate correctly. This supply voltage is termed the "marginal voltage." For a particular device (bipolor or MOS) the marginal voltage for different input words should not vary significantly if the device is defect free. Marginal voltages which fall outside the normal range are termed "anomalous" and may be associated with a specific latent defect. When marginal voltage analysis is combined with a stimulation source it provides a non-destructive, non-contacting technique for locating faults in integrated circuits. The stimulation source causes a shift in the "marginal voltage." The area of the chip that is being stimulated when the "marginal voltage" shifts is the probable defect location.

This effort is mainly concerned with the efficient and non-destructive location of faults once they are detected using marginal voltage analysis. The accomplishments of this effort are: (1) a laboratory marginal voltage analysis system has been constructed, (2) three illumination techniques (spot, strip, flood) were evaluated, (3) for the stimulation source a hybrid instrument which is a scanning electron microscope incorporating an optical scanning system was described and demonstrated, and (4) a case study was performed to locate faults in an integrated circuit.

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EVALUATION

This effort was mainly concerned with the efficient, non-destructive location of faults in integrated circuits once they are detected using marginal voltage analysis. Marginal voltage analysis combined with device surface stimulation (E-beam or optical source) has been shown to locate defect sites in integrated circuits. The original technique required that the stimulation source be raster scanned across the device. For a large device the testing time could become prohibitive since every micrometer of the device would have to be scanned. A more efficient search method was investigated under this effort which would allow a shorter time to locate the defect site by the use of flood illumination.

This effort has demonstrated that marginal voltage analysis combined with flood illumination can be an efficient and non-destructive technique for locating faults in combinational integrated circuits. It should be cautioned though that there is a possibility that the flood illumination may not always locate the fault or faults in a circuit. This is because certain faults exhibit an increase in marginal voltage while others a decrease when illuminated. If two competing faults are illuminated at the same time they may mask each other. Alternate search methods (strip or spot illumination) mode would then have to be used.

Additional work still needs to be done in the area of locating defect sites in integrated circuits. As circuits become more complex the problem of locating defects increases proportionally. This technique is a possible solution to the problem but a more rigorous analysis is needed in the type of defects that are detectable, how the defects affect the marginal voltage, and how this technique can be applied to large sequential circuits. Additional research should be done to address these problems.

Mark T. Pronobis

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SUMMARY

Marginal voltage analysis is a technique for testing complex integrated circuits and shows promise for locating latent defects without access to the manufacturer's CAD (Computer Aided Design) software. The supply voltage at which a circuit just fails to operate correctly for a particular input word is termed the 'marginal voltage'. For a particular device, whether bipolar or MOS (Metal-Oxide-Semiconductor) the marginal voltages for different input words should not vary significantly. Marginal voltages which fall outside the normal range are termed 'anomalous' and may be associated with specific latent defects or poor circuit design with insufficient noise margins. These types of circuit 'weak spots' may, in principle, be differentiated by comparing nominally identical devices from the same batch and then from different batches. The distribution of marginal voltages is intimately related to the degree to which the manufacturer has his process under control.

The present work is concerned principally with the efficient, non-destructive location of such faults once they are detected using marginal voltage analysis. When the circuit is stimulated using an electron or optical beam, there is a shift in marginal voltage, and therefore weak spots associated with anomalous marginal voltages may be located. The advantages and disadvantages of using electron beams and optical beams are considered, and the use of a hybrid instrument, the ERA SOMSEM, is considered and subsequently demonstrated.

The marginal voltage characteristics of simple gates are discussed in terms of the measurement impedance and its effect on hysteresis. Hysteresis effects represent a problem for automated testing systems. The marginal voltage shift produced by different stimulation sources is considered together with the types of defect which may be located. The relative efficiencies of different search formats, such as raster scanning and the binary search, are compared both theoretically and experimentally. Two case studies of combinational devices with anomalous marginal voltages are reported, one for TTL and the other for CMOS technology, and the defective areas were successfully located using the different search formats.

The extension of these techniques for defect location in sequential circuits is discussed and finally recommendations for further work are made, based on the principal conclusions.

CONTENTS

1 BACKGROUND

Adequate testing of complex digital microcircuits is of paramount importance in both military and civilian applications to manufacturer and user alike. Ideally, automated testing should not only indicate faulty circuits, but also circuits with latent defects. Also, in order for the device manufacturer to take remedial action to improve yield in subsequent batches, the testing procedure should reveal the location of the defects.

Whilst it is true that procedures for the location of a defect within the microciruit are, in principle, contained within the manufacturer's Computer Aided Design (CAD) software in combination with functional tests, the CAD is proprietry and not generally available. In any case, direct monitoring of the waveforms at internal circuit nodes, remote from the input and output pins, is preferable. Furthermore, in failure analysis an imaging technique is required to both locate and characterise the defect.

These considerations have promoted much interest in automated testing procedures which combine an imaging technique with an electrical test. Attention has focussed mainly on the use of the Scanning Electron Microscope (SEM) in the stroboscopic voltage contrast mode (see for example Ref.1) whilst the circuit is being exercised. Although the interrogation of each circuit node of a complex microcircuit is feasible, in terms of the spatial resolution capability of the SEM and also the voltage resolution of the detection system itself, the technique is not practicable for routine testing. This is partly because of protracted testing times, and the resultant likelihood of radiation damage from the electron beam, and partly because, without great care in system design and operation, information from neighbouring nodes interferes with the nodal waveform under observation. This problem is likely to be exacerbated by the advent of multilayered metallisations and ever-smaller device dimensions.

The problem of electron beam damage, which is particularly severe for Metal Oxide Semiconductor (MOS) devices, may be circumvented by using a laser beam to interrogate circuit nodes, as has been demonstrated by RADC (Ref.2 and Ref.3), both for timing analysis of individual nodes and location of latch-up failure sites in CMOS devices. Surface potentials are not, of course, measured. A comprehensive device analysis system based on laser scanning techniques has been developed by

Nagase (Ref.4) using two lasers of different wavelengths, one more penetrating than the other, to image device operation at difference depths below the silicon surface.

A recent development in scanning optical microscopy is the SOMSEM (Ref.5) an SEM-based Scanning Optical Microscope which avoids the problems inherent in mechanically-scanned, laser-based systems, and takes advantage of the well-developed image processing capability of the modern SEM. When regarded as a hybrid instrument, the SOMSEM has the potential for non-destructive optical evaluation of MOS devices followed by failure analysis using electron-beam techniques.

Various forms of functional testing (as distinct from direct verification of internal circuit nodes) have been proposed which are compatible with imaging systems to reveal defect sites. Output words from the device-under-test (DUT) are compared with those from a correctly operating device or a truth table stored in a memory. In order to interface the error signal with the imaging system for location of the origin of the defective output word, the imaging system itself, or some stimulation technique in registration with it, must have a measurable effect on circuit operation. For example, in the laser die probing technique (Ref.2), the supply current to the DUT is monitored while a chopped laser beam is incident on the drain junction of an individual transistor. If the corresponding variations in supply current to the CMOS device are high, then the transistor is off, and if the variations are low the transistor is on. This technique can be used to verify the state of each transistor as it turns on and off as a result of successive clock pulses.

One form of functional testing, known as Marginal Voltage Testing (Ref.6), can be combined with an imaging technique to locate 'weak spots' in the DUT. These areas may be defective because of circuit design or because of processing defects. The principle of marginal voltage testing for combinational circuits (where the output word is a function of the input word only, there being no clock pulse or storage effects) is as follows.

For each input word, the corresponding output word is monitored as the supply voltage is moved outside the manufacturer's specified normal working range. The supply voltage at which the circuit ceases to operate correctly (i.e. the output word becomes incorrect) is known as the 'marginal voltage' for the particular input

word. The measured values of marginal voltage tend to be all rather similar, say within 10% of each other for the lower marginal voltages and similarly for the upper values, but occasionally anomalous values are obtained which are significantly different. An 'anomalous marginal voltage' may be indicative of a circuit design fault, or a processing variation (in which case circuits from the same batch may well exhibit the same anomalous values) or a defect peculiar to that particular device. Thus marginal voltage testing is a potentially powerful technique which can be used, in principle, to identify abnormal devices at various stages in the development of a new integrated circuit, ranging from circuit design verification through process optimisation and beyond for batch sampling or even routine screening.

In practice, binary search procedures are used to determine the marginal voltages since testing speed is very important and the marginal voltage is measured for every input word. The upper marginal voltages are generally not measured because of the possibility of damaging the device. Furthermore, before testing begins, the minimum high and the maximum low logic levels must be set. These definitions will in general be different for different silicon technologies.

Although marginal voltage measurements are potentially useful indicators of reliability and are also closely associated with the important concepts of 'noise margins', they do not in themselves locate the origin of the circuit weak spots. However, when the DUT is at the marginal voltage corresponding to a particular input word, it is in a finely balanced condition by definition, and additional stimulation in the form of a beam of electrons or light can alter this balance and change the output word. The position of the external stimulation when this happens then corresponds, in principle, to the site of a weak spot, and the British Telecom work (Ref.6) has shown that anomalous marginal voltages are often associated with defects in bipolar devices. Note that the defects themselves do not have to be activated by the external stimulation - a change in anomalous marginal voltage is sufficient for defect location (see Section 3.2). Both scanning electron beam and scanning light spot techniques were used. One of the principal objectives of the present work was to extend these studies to CMOS devices, which would be damaged by an electron beam, using a more sophisticated scanning optical system.

The basic premise of marginal voltage testing is that anomalous marginal voltages are symptomatic of defects, and that there is a correlation between yield and

reliability. This philosophy is expanded in Ref.7 and is the subject of an associated work program at ERA, whereas the main emphasis of the present work is on the location of defects. The work described in this report starts with the marginal voltage behaviour of simple gates in both bipolar and MOS technologies and progresses to the location of circuit 'weak spots' in a more complex device using the projection of light onto the DUT in different test patterns. The efficiency of the different search formats is discussed and also the types of locatable defects. Defect location is demonstrated in two case studies - a CMOS adder and a TTL comparator. The use of the SOMSEM as the source of external stimulation for marginal voltage studies is demonstrated for simple CMOS devices. Finally, the extension of the search procedures to complex sequential circuits is discussed.

2 MARGINAL VOLTAGE CHARACTERISTICS

2.1 Introduction

Before defect location can be attempted in relatively complex circuits, it is necessary to understand the normal marginal voltage characteristics of simple gates and their dependence on measurement conditions. In this context, the term 'marginal voltage characteristic' is defined as a plot of gate output voltage against supply voltage for the two binary states of the output with the inputs strapped to either power rail, although strictly the complete truth table should be examined. In practice, however, we have found that the MV characteristics of normal simple gates are not affected by the precise input words except insofar as the gate outputs are placed in one of the two possible states. (This would not necessarily be the case, of course, for anomalous marginal voltages which, by definition correspond to particular input words).

The gates chosen for investigation were of the dual input variety with four gates on the 14-pin device. The gate types consisted of the TTL 7400 series (including NAND, AND and EXOR gates) and the CMOS 4000 series (including NAND, AND, OR and NOR functions). A limited number of high-speed CMOS gates from the 5400 series were also tested. The advantage of having four identical gates on one device was that results could easily be checked for consistency. In fact the spread of marginal voltage values for a given device was less than 100 mV, although more significant variations were encountered from batch to batch and for different manufacturers for the same device type. For different device types, however, considerable variations were found in the marginal voltage characteristics and it was necessary to automate the measurements to obtain an overall picture of marginal voltage behaviour. Only one gate was found to be abnormal in more than one hundred, and this was from the high-speed CMOS family.

A block diagram of the measurement system is shown in Fig.1. The HP 6002A programmable power supply is controlled by the HP 9826 personal computer, and the gate output from the DUT is measured using a DVM. The results are recorded using a digital plotter (HP 7470A) for the range of supply voltage (0-5 V) in one hundred incremental steps, taking a few minutes to measure each MV characteristic. The direction of change of the supply voltage could be reversed,

either to check the previous measurements or to measure the MV characteristic for a different input word or gate. The software for the test procedure was written in Basic with disc storage, and the interfaces were of the IEEE 488 family.

The principal trends in marginal voltage behaviour are now illustrated with a selection of gates and combinations of gates.

2.2 Effect of Measurement Impedance and Hysteresis

The basic marginal voltage characteristics for a CMOS NAND gate are shown in Fig.2. At approximately 1.3 V the nominal high level gate output starts to fall rapidly (whether its origin is due to input words 00, 01 or 10) and becomes indistinguishable from the logic low level output at about 1.2 V. This general behaviour is observed for all CMOS gates, although the precise values may vary, and, of course, the input words producing logic output '1' will depend on gate type.

The degradation of the logic output 'high' is related to the values of the threshold voltages for the p-channel and n-channel transistors and between 1.2 and 1.3 V none of the four transistors comprising the gate are fully on or fully off. This makes interpretation difficult, but it should be remembered that anomalously high values of marginal voltage will ensure that the vast majority of the transistors of a complex device would be either fully on or fully off, the remaining transistors being associated in some way with the anomalous marginal voltage and, by implication, in the vicinity of the defect responsible.

From Fig.2 it can also be seen that the gate output low level (obtained in this case for input word 11) remains unchanged as the supply voltage is decreased. In this case, no definition of marginal voltage is possible, and this is frequently the case for one or other of the output states. However, the lack of a well-defined marginal voltage for a particular state of an individual gate does not invalidate marginal voltage testing and defect location for complex devices containing many such gates in different conditions. Furthermore, external stimulation, e.g. from a laser beam or SEM electron beam has a profound effect on MV characteristics as discussed in Section 3 below.

One important consideration for CMOS devices is the effect of 'loading' on the output stages of gates. In a complex device containing many gates each gate

presents virtually infinite impedance to the preceding gate. In order to simulate this condition, the DVM (with input impedance 20 M_Ω) was replaced by a Keithley Electrometer with an impedance greater than $10^{10}{}_\Omega$. As shown in Fig.3, the marginal voltage associated with the logic level high output shifts somewhat, and the shift may be positive or negative depending on the particular gate type being examined. The effect of measurement impedance is particularly important for nominal logic level low outputs in the presence of illumination (see Section 3).

More complex devices may be simulated by cascading two or more simple gates as shown in Fig.4 and Fig.5. The results of such measurements may be understood qualitatively in terms of the basic characteristics such as those shown in Fig.2 and Fig.3, but with the additional complication that there is a dependence on the direction of change of the supply voltage. This is thought to be due to the retention of charge by the input capacitance of the following gate causing the gate output to 'stick' in a particular state until the charge has leaked away. Other possible combinations of inputs gave similar results (relative to the appropriate truth table) but it should be remembered that so far we are considering normal gates only.

In the case of TTL gates, the effect of measurement impedance is minimal, as would be expected since these gates are capable of sinking considerable currents at the output stage. The MV characteristics for a relatively complex gate - the EXOR 7486 - are shown in Fig.6. No hysteresis effects are apparent for TTL gate combinations because of the low input impedances involved.

2.3 Implications for Automated Testing

The presence of hysteresis effects casts doubt on the validity of the binary search technique for finding the marginal voltage, which was the technique used by British Telecom in their investigation of TTL devices (Ref.6). There are other problems associated with a binary search for the marginal voltage (not to be confused with the binary search for defect location - see 3.4 later). Consider Fig.7 which shows a marginal voltage characteristic for three CMOS NAND gates linked in a simple inverter chain. Over a narrow supply voltage range (1.0 to 1.3 V), the nominal logic output 'LOW' reaches a maximum and this would confuse a binary search for the marginal voltage unless additional safeguards were built into the software.

Other CMOS gates and gate combinations show similar behaviour with respect to hysteresis and measurement impedance, but a dependence on measurement impedance is not observed in all cases. The behaviour of TTL gates is relatively simple (see Fig.8 for another example) because of the comparatively low impedances, but nevertheless the binary search for the marginal voltage may be thwarted by a characteristic such as that shown in Fig.9 for two successive TTL gates unless precautions were taken. No specific reference to this problem is made by British Telecom in their original paper (Ref.6), but it may be that their choice of PASS/FAIL threshold levels avoided such problems.

A convenient choice of PASS/FAIL threshold levels, particularly for CMOS devices, is shown in Fig.7. When the logic level 'low' rises to more than one third of the supply voltage a FAIL condition is reached. Similarly, we define a FAIL for the logic 'high' level when it falls below two-thirds of the supply voltage. Clearly a straightforward binary search procedure would not converge to the marginal voltage associated with the logic level 'low' at around 1.2 V for the case of the characteristic shown in Fig.7.

2.4 Different Manufacturers

Further examples of marginal voltage characteristics for three different CMOS gate types are shown in Fig.10, Fig.11 and Fig.12. The logic output 'low' level is not shown, since it remains at zero volts in each case as for the NAND gate in Fig.2.

Devices from four different manufacturers were assessed - RCA, National Semiconductors, Motorola and Mullard (HEF). There is a considerable spread in marginal voltage, ranging from about 0.8 V to 1.5 V, whereas the spread for an individual device with four gates is less than 0.1 V. Whilst each manufacturer has a different circuit layout for the same gate function, it is probable that the range of marginal voltages is associated with a range of threshold voltages rather than specific circuit design. Thus for a given manufacturer, variations would exist from batch to batch, and this may well be indicative of the degree to which the process is under control.

3 EFFECT OF EXTERNAL STIMULATION

3.1 Marginal Voltage Shift

The basic marginal voltage characteristics of Section 2, have been remeasured for devices exposed to various light sources. Ceramic packaged devices were chosen because they can be opened easily.

As British Telecom pointed out in their original paper (Ref.6) bipolar devices are very insensitive to light. They estimated that the luminous intensity of their 50 μ square spot (produced from the tungsten filament lamp and a microscope objective) was 10^7 lux and that this induced a marginal voltage shift of between 5 and 50 mV for TTL. In terms of power density, this luminous intensity corresponds to several watts per square centimeter. Using an expanded laser beam, we have measured a marginal voltage shift of 0.5 mV for a 7408 AND gate at an intensity of 200 mW cm^{-2} (this was calibrated using a Centronix photodiode). These results are in broad agreement, but they also show that defect location in bipolar technologies using marginal voltage techniques is only feasible for very high intensity light sources, and different search formats, such as those described in 3.4 below, may not always be practicable. In any case, since electron beam techniques are capable of higher resolution, and bearing in mind that for bipolar devices beam damage is not a severe problem, it is much more attractive to use the SEM for such studies, as demonstrated at British Telecom. However, the SEM is limited to the 'spot scan' search format.

The situation is very different for MOS devices. Even low light intensities have a profound effect on the marginal voltage characteristics, particularly when gate outputs are virtually open circuit, as in a complex device. Consider, for example, the behaviour of the CMOS NOR 4001 gate for the case of a nominal logic output 'low'. When measured in dark conditions, the output remains at zero for all values of the supply voltage, whereas Fig.13 clearly shows how the output rises for supply voltages below about 1.5 V for the RCA device and about 1.1 V for the National device when measured under the same illumination conditions. (The term 'RED' on this and subsequent figures refers to particular illumination conditions equivalent to about 100 μW cm^{-2}). Similarly (see Fig.14), when the nominal gate output is high, and the supply voltage is below the marginal voltage (thus producing zero output in the dark) the output rises under illumination conditions, and follows

essentially the same path as the MV characteristic for a device in the dark when measured in the direction of decreasing supply voltage (Fig.5). In other words, illumination duplicates the hysteresis effect referred to previously.

In a sense, the presence of illumination removes the well-defined marginal voltage from the logic output 'high' characteristic but on the other hand adds a well-defined marginal voltage to the logic output 'low' characteristic. Even this is an over-simplification since the intensity of illumination is also important. For example, Fig.15 shows the MV characteristics of a CMOS 4071 gate under very low illumination conditions (about 10 $\mu W\ cm^{-2}$). As the intensity is increased, the marginal voltage for the high output condition decreases whereas it increases for the low output condition. This opposing tendency may have important consequences when comparing search formats, as in 3.4 below.

The marginal voltage shift for CMOS devices has been measured as a function of light intensity for a simple device and for a more complex circuit - the CMOS 4008 adder, investigated in Section 4 below. The arrangement of two CMOS NAND gates shown in Fig.5 was used for the basic assessment with the second gate acting as a buffer so that a DVM could be used to monitor the logic output 'high' without the hysteresis effects associated with the electrometer measurement. Under these conditions, it is the first gate which is responsible for a shift in marginal voltage and the result is shown in Fig.16. Between 10 and 100 $\mu W\ cm^{-2}$ the marginal voltage shift increases by a factor of between two and three, and another order of magnitude increase in intensity brings a slightly greater increase, but the shift is still markedly sub-linear with respect to intensity, implying some saturation mechanism, such as the charging of a capacitive element. A convenient working point is 100 $\mu W\ cm^{-2}$, giving rise to an easily-measured marginal voltage shift of 100 mV in simple devices. We shall see later in Section 4 that more complex devices require rather higher intensities.

3.2 Locatable Types of Defect

In order to locate a defect using marginal voltage techniques, it is necessary for the defect to give rise to an anomalous marginal voltage i.e. a supply voltage (corresponding to a particular input word) which is significantly higher than the norm for other input words. Under these circumstances, as the supply voltage is progressively reduced the first part of the circuit to cease operating correctly is

the defective part. By definition the defective part gives rise to the anomalous marginal voltage, and if light or an electron beam affects the anomalous marginal voltage the defect is locatable, at least to the extent that the part of the circuit responsible for an incorrect bit or bits in the output word is located. If, in addition, the defect itself is 'optically active' rather than simply giving rise to an anomalous electrical characteristic, then the location will be more precise. Otherwise, the defect would be locatable to within a gate or two. We can thus compose a list of locatable defects comprising two categories; those defects which would be specifically detected using OBIC or EBIC methods once the general area of the fault was found, and those detectable only through their influence on the marginal voltage measurement or other purely electrical test.

In the first category we would expect to find defects such as precipitates (giving rise to leakage paths in junctions), recombination centres, stacking faults etc. Such defects may be located using OBIC and EBIC (or even luminescence) if the defective area is first approximately located, e.g. to within a few tens of microns, using marginal voltage analysis combined with external stimulation, whereas normally these techniques are insufficiently sensitive when applied to a complex device. The finely balanced marginal voltage condition for a given input word should greatly increase the sensitivity of OBIC for CMOS in particular since the quiescent supply current is so low compared to that induced by a switching gate.

In the other category are essentially passive defects such as masking faults which affect the dimensions of a particular element which in turn gives rise to an anomalous marginal voltage. Fluctuations in substrate resistivity may also result in anomalous marginal voltages and to areas which, although locatable, do not contain a specific defect but rather an element or elements out of the normal specifications. In such cases, for CMOS, the nearest output transistor which is 'off' will be the sensitive area detected. Other examples of passive defects are pits, scratches and ionic contaminants in the surface oxide giving rise to localised variations in threshold voltage.

3.3 Comparison of Stimulation Sources and Spectral Response Considerations

In addition to the lack of beam damage, the optical stimulation technique has an important advantage compared with electron beam testing. By varying the wavelength of the incident light, different depths of silicon may be probed

depending on the absorption coefficient at that particular wavelength - see Fig.17 - and the simple De Beer's relationship:

$$I_x = I_o \exp - (\alpha x)$$

Where I_x is the intensity at depth x, I_o is the intensity at the surface and is the absorption coefficient of silicon for the wavelength of radiation used.

Changing the beam voltage of the SEM also allows stimulation at different depths, as Fig.18 shows, but the scope for such investigations is considerably reduced. The ionization profiles of Fig.18 were calculated using the method of Everhart and Hoff (Ref.8). It is generally accepted that MOS devices survive a radiation dose of less than 10 k Rads which, for typical SEM operating conditions, would take only 0.5s. For comparison the electron-hole pair generation rates for two light wavelengths are shown in Fig.19. Blue light at 450 nm is at present used in the SOMSEM because of the availability of a fine-grained P11 phosphor. The other wavelength of particular interest is red light at 632 nm - the principal wavelength of the Helium-Neon laser, which is a convenient high-intensity laboratory source for the optical stimulation experiments.

In practice the penetration depth of the high energy electrons of the SEM in silicon integrated circuits will be severely reduced by any passivating layers, whereas these are normally transparent to light. This is a distinct practical advantage of optical techniques since no special preparation is necessary. In fact it is possible to visualise automated testing on packaged devices with transparent lids, although for normal operation they would be blacked-out.

In order to determine the optimum wavelength for stimulation of silicon ICs, the spectral response for the optical beam induced current was measured for CMOS technology, using a Rofin rotating grating monochromator and an Analogic D6000 Waveform Analyser controlled by an HP 9826 Desktop Computer. The grating rotates at constant speed so that spectral responses are obtained very rapidly, albeit somewhat approximately, and can be displayed on an oscilloscope because of the repetitive nature of the signal. The D6000 Waveform Analyser incorporates a digital storage oscilloscope and various signal processing functions so that the repetitive spectral response can be averaged over, say, 32 sweeps to improve the signal-to-noise ratio.

The throughput of the monochromator was measured with a silicon detector manufactured by SDC. The spectral response of the silicon photodiode was extracted from the manufacturer's data sheet using a digitising routine (see Fig.20), and this curve was used to obtain the throughput of the monochromator under particular illumination conditions (the intensity of the calculated throughput is shown in Fig.21). This calculated throughput was subsequently used to normalise the experimentally obtained OBIC spectral response of an MOS device and the normalised response is shown in Fig.22. It can be seen that over the visible and near IR part of the spectrum the optical beam induced current does not vary greatly until about 850 nm when the silicon absorption edge starts to have a significant effect. This is despite the fact that the absorption coefficient is changing rapidly throughout the range, but carriers generated within a diffusion length of the collecting junctions and electrodes will contribute to the OBIC signal. At longer wavelengths, carriers are generated deeper in the device because of the lower absorption coefficient, and many of these carriers will not contribute to the OBIC signal. Under marginal voltage conditions, the spectral response associated with a logic gate output zero was obtained (see Fig.23). The flat part of the response extends to about 900 nm and a much steeper fall-off is observed than for the OBIC spectral response. The response corresponding to a logic gate output '1' is very similar to that shown in Fig.23. The spectral responses associated with different parts of the circuit may be expected to differ because of their varying depths below the surface. The periodicity evident in Fig.22 may be due to an interference effect in the passivation layer.

From these measurements, it can be inferred that the marginal voltage shift for normal (working) CMOS devices is not critically dependent on wavelength over a considerable wavelength range. The same applies to the OBIC signal. Thus phosphor selection for the SOMSEM may be made on the basis of other factors such as efficiency, grain size, burn resistance etc. However, anomalous marginal voltages, which are related to defects, may be expected to have different spectral dependences depending on the precise nature of the defect, just as different parts of the circuit have different spectral responses. This could be the basis of a procedure for identifying and characterising defects without applying destructive failure analysis techniques. In this context, defect location may play a secondary role, and such measurements could be useful for monitoring fabrication processes and comparing batches of ICs. It would first be necessary to establish correlations between fingerprint spectral responses and device performance, however.

3.4 Comparison of Search Formats

The simplest way of stimulating the device in the marginal voltage condition is one point at a time in a raster pattern. The SEM is, of course, ideal for this purpose as is the SOMSEM. However this sequential search is time-consuming if a large number of locations are to be addressed - say a 1024 x 1024 matrix giving a resolution of 10 μ on a 1 cm x 1 cm device. In the worst possible case, more than one million sites have to be tested to locate a defect.

A more economical search pattern is the XY strip location technique where the defect is located at the intersection of two line scans. This search, for the worst possible case, would require a maximum of 1024 iterations for the X location and 1024 for the Y co-ordinate, giving 2048 iterations in all. However, the most economical testing method would be provided by a binary search format which would require about twenty iterations to locate a defect ($2^{20} \sim 10^6$).

Experimentally, these search formats may be conveniently studied using a set of 2^n projection slides with appropriate patterns within a 4 x 4 matrix. The complete mask set is shown in Fig.24 and the projection system is shown in Fig.25. The laser beam expander used without spatial filtering (which requires costly precision optical components and critical alignment) results in a considerable amount of 'speckle'. Uniformity of illumination is important for the search formats, particularly when many parts of the device are illuminated simultaneously. Consequently a tungsten filament lamp, which produces a more uniform brightness, was used in cases where the illumination intensity was not of paramount importance (see Fig.39 for the appropriate optical bench layout).

The number of mask patterns required for each search format is not directly related to the maximum number of iterations required as Fig.24 shows. For example, for the raster search format the sixteen possible locations of the light spot requires only three masks, but these must be rotated and/or inverted for the entire scan. Similarly, the X-Y strip location method requires only two masks, and the eight patterns are obtained by rotation and inversion. Finally, the bottom six patterns of Fig.24 are used for the binary search and it is clear that there is some redundancy depending on how the illuminated area is halved for the next iteration. This redundancy has been used to check the locations of circuit weak spots as detailed in Sections 4 and 5 below.

4 CASE STUDY FOR CMOS ADDER

4.1 Introduction

Whilst simple combinations of dual-input gates are useful when extrapolating basic marginal voltage characteristics to obtain an understanding of the behaviour of complex devices, they are not sufficiently complex to develop the concept of circuit 'weak-spots'. By 'weak-spots' we mean those areas of a device which are most sensitive to external stimulation when under marginal voltage conditions, either because of inadequate noise margins in circuit design or because of process variations and specific defects. In order to demonstrate the location of such areas, a relatively complex device was found to be necessary and the MSI (medium scale integration) 4008 CMOS 4-bit full adder was chosen because it is one of the more complex combinational circuits readily available.

4.2 MV Characteristics

The CMOS 4008 adder device may be used to add two 4-bit input words and a 1-bit word (a 'carry' from, say, a previous adder) and produces a 5-bit output word. For marginal voltage testing purposes, it may be treated as a device which produces a 5-bit output word in response to a 9-bit input word, although, of course some of the 9-bits are interrelated.

For a particular input word (the binary equivalent of 501) the MV characteristics of each of the output bits were measured in both light and dark conditions, and with low and high impedances. The input word was inverted (i.e. zeros to ones and vice-versa) and the characteristics remeasured. From this considerable amount of data, certain comparisons may be made with the MV characteristics of simple gates or gate combinations.

The principal features may be illustrated with reference to Fig.26, 27, 28 and 29 showing both low and high impedance measurements for nominal low and high logic state outputs. The measurements are accurately reproducible despite the occurrence of apparently spurious points which are highlighted by the choice of a larger incremental voltage (to reduce testing times) than that selected for the data on simpler gate configurations. The effect of illumination is broadly similar and can be understood qualitatively in terms of combinations of more basic

characteristics. Anomalous marginal voltage characteristics would be expected to be much simpler because the anomalous area would dominate the characteristics for the reasons discussed in Section 3.4 above.

4.3 Locations of Circuit Weak Spots

By illuminating the entire device and monitoring an output word as a function of intensity for supply voltages near the marginal voltage, it is easy to demonstrate that the number of errors in the output bits increases as the intensity increases, and decreases with an increase in supply voltage. A simple pictorial representation of these trends is shown in Fig.30. In the finely-balanced marginal voltage conditions, errors caused by an increase in external stimulation must be counteracted by an increase in supply voltage.

The areas responsible for output errors under illumination conditions may readily be located by the simple 'spot scan' or raster search format, and typical results are shown in Fig.31. The intensity is adjusted to the minimum required for output errors. The correct output word is 11010, but for two of the sixteen squares of the grid array the output word has errors. It must be inferred that these two areas contain gates which are more 'marginal' (i.e. furthest away from their correct operating points and with poor noise immunity) than gates in the remainder of the device. For this value of intensity, an increase in supply voltage of 100 mV returns the output word to its correct form.

The X-Y strip search format was equally successful in locating the two circuit 'weak spots' and the output word for the eight possible positions of the illuminated strip is shown in Fig.32. The same two 'marginal' squares are located, although in one case one of the output bits has been labelled '½' because it was neither fully high nor fully low.

The binary search was also successful in locating the 'marginal' squares but again one particular illumination pattern produced the same dubious bit as before and indicated another weak spot. The results are shown in Fig.33, and a number of 'redundant' iterations are included by way of confirmation.

Further studies have confirmed these findings and have also demonstrated the importance of selecting the lowest intensity required to give a positive result in

the search. If this procedure is not followed, numerous 'marginal' areas of the device may be located, some arising from combinations of others, and this confuses the more sophisticated search patterns where more than one marginal area may be illuminated at any one time.

Experiments such as these serve to demonstrate that essentially the same 'weak spots' may be located using the different search formats, with obvious implications for automated testing. Furthermore, the detection of such 'marginal' areas is clearly more difficult for the normally-operating devices examined thus far, since devices with anomalous marginal voltages would be expected to contain marginal areas at significantly higher supply voltages, by definition. Since the remainder of the circuit would be operating normally, such areas would be comparatively easy to find. This has now been verified for a TTL comparator (see Section 5 below) and for the CMOS adder.

4.4 Location of Irradiated Sites

It is well known that ionizing radiation induces a threshold shift in MOS devices. The SEM can be used to irradiate devices in a localised fashion if care is taken not to damage the remainder of the circuit. This provides a means of testing the efficiencies of the different search formats in locating the defect sites.

The irradiation of simple gates using both the SEM and Co60 γ ray source has shown that marginal voltage shifts are induced in MOS devices. This provides indirect evidence for the link between threshold voltage and marginal voltage. For NAND gates, ionizing radiation reduces the marginal voltage by several mV for a few k Rads total dose. This reduction, rather than an increase, makes such devices unsuitable for a comparison of the defect location techniques.

In order to produce a realistic defect on a more complex device, RADC agreed to irradiate localised sites on CMOS adders. For two of the three devices (designated No.6 and No.7) supplied for evaluation, the radiation induced very large changes in the marginal voltages - from 1.3 V to 17 V. These devices could not be measured on our automated MV test rig because the comparator circuitry is limited to 5 V. However, sufficient results were obtained from the remaining device (designated No.2) to show that a fault was associated with inputs A1 and B1 (pins 6 and 7) when both inputs were high.

The device was transferred to the optical assessment rig described in Section 3.4. The marginal voltage for the suspect input word was found to be 10.8 V, whereas other input words had marginal voltages between 1.5 and 3.7 V. Since, normal (unirradiated) devices have marginal voltages of approximately 1.5 V, this indicates that other parts of the circuit were inadvertently irradiated. However, the anomalous marginal voltage of 10.8 V is sufficiently high to ensure that all parts of the circuit other than the part addressed by input pins 6 and 7 are in their correct, saturated condition.

Under marginal voltage conditions, using the projection of the 4 x 4 matrix patterns described in Section 3.4, the defective area was found to be near the bond pads to pins 6, 7 and 8 (see Fig.34). Pin 8 is the ground pin. All three search formats were successful in locating the area, and the level of illumination used produced a 10 mV decrease in marginal voltage.

With further development of the optical projection system, more iterations of the binary search would be possible so that more localised areas could be addressed. One approach is to decrease the size of the projected patterns and to incorporate a means of registering these patterns with a conventional reflected image of the device. It should be pointed out that relatively high light intensities were necessary for the location of the defective area in all three search modes, and that the ERA SOMSEM in its present state of development would not have sufficient intensity for defect location in these more complex devices.

5 CASE STUDY FOR TTL COMPARATOR

5.1 Introduction

During the latter half of this contract, an associated work program was launched which was designed to find the correlation, if any, between anomalous marginal voltages and reliability. Preliminary work at British Telecom has suggested that this is the case, and the work in progress at ERA has produced some devices with anomalous marginal voltages, but the failure rate is very low. Here we consider one particular device which developed an anomalous marginal voltage during an accelerated life test.

The background to the marginal voltage measurements and the accelerated life tests is as follows. Preliminary marginal voltage measurements, using a condensed truth table, were made on one thousand TTL comparators (National Semiconductor).

A pattern of 14 input words, which were selected to address all the principal functions of the 4-bit comparator, was cyclically imposed on each device as the supply voltage was progressively reduced. The supply voltage at which each device first failed this simplified marginal voltage test was recorded together with a device indentification number. This supply voltage therefore corresponds to the word with the highest value of marginal voltage for the test sequence.

Out of these 1000 devices, two groups of 50 were selected, one of which contained devices with the highest values of critcal supply voltage, whilst the other group contained those devices with the lowest critical values. Furthermore, the two groups were both ordered in terms of these critical values, i.e. the devices with the highest value is designated No.50H the device with the next highest number 49H etc (see Fig.35). Similarly, for the fifty devices with the lowest operating voltages, the devices were designated No.1L, 2L etc., and the gap between the critical values of supply voltage for No.50L and No.50H was only 190 mV whereas the gap between 1H and 1L was 1.84 V. For the L group, the spread of marginal voltage values was very much smaller than for the H group - 60 mV compared with 1.59 V.

These principal features are illustrated in Fig.35 and vindicate the basic premise of marginal voltage philosophy i.e. good devices have well-defined limits of operation

with very little spread. Conversely, the class of 'poor' devices contains much more variation. Whether high values of marginal voltage constitute a reliability hazard is still an open question, although it is clearly preferable for systems engineers to choose the devices with low values since they have higher noise margins and have more closely defined parameters.

Accelerated life-tests were conducted at 180°C with 5 V supply voltage and a fixed input word. After 72 hours, device No.50H was drawing excessive supply current (0.09 to 0.15 A instead of the normal 0.075 to 0.1 A) particularly for an input word corresponding to A_0 or B_0 low.

5.2 Location of Circuit Weak Spots using the SEM

The defective device was removed from the accelerated life-test program and examined using the SEM in the voltage contrast mode. Comparing voltage contrast micrographs obtained for a normal device and the suspect device under the same supply voltage conditions (below the marginal voltage for the suspect device) showed a faulty area associated with the inputs A_0 and B_0 (see Figs.36-38). Below the marginal voltage the output corresponding to A_0 and B_0 does indeed register a logic error. At the marginal voltage this output was fed into the input of the SEM through a 1 MΩ resistor in order to produce a 'logic state map' showing the particular part of the circuit, which, when excited by the electron beam, gives rise to a large change in the output pin voltage. Thus the final image (Fig.39) consists of an electron beam induced voltage image (for pin 5) obtained under marginal voltage conditions such that the marginal areas are superimposed. Whilst the contrast of the EBIV (electron beam induced voltage) image would be expected to be approximately linearly dependent on the supply voltage, the superimposed logic state map has a critical dependence near the marginal voltage. Consequently, the features associated with marginal voltage conditions are easily identified, especially if image subtraction techniques are used, and, for the present study, the area found is near to the area highlighted using the voltage contrast technique. Both areas are associated with the inputs A_0 and B_0 and the corresponding output, pin 5. Fig.39 also demonstrates how critical the optimum supply voltage is for imaging the defective part - incorrect selection will result in an extended band across the slice - there is also an optimum scan time.

Fig.40 shows similar images of the same area but for a normal device. Areas in addition to the previously located weak spot are highlighted but at a lower value of

supply voltage (about 3 V). The range of supply voltages spans only 100 mV and yet the detail revealed in these logic state maps near the marginal voltage changes markedly. Achieving 20 mV resolution with voltage contrast techniques is notoriously difficult, and we believe that marginal voltage techniques offer a realistic alternative.

5.3 Location Using Different Search Formats

The SEM itself does not allow the implementation of different search formats, although it is possible that the SOMSEM, used with long-persistence phosphors, would allow the location of circuit weak spots in CMOS devices using a binary or strip location search. However, the existence of a bipolar device with an anomalous marginal voltage gave the opportunity of comparing the different search formats which had previously only been applied to normal CMOS devices and the CMOS adder which had been deliberately damaged.

As predicted in Section 4 above, the location of the circuit weak spot was easier in the anomalous device than in normal devices because the defective area is revealed against a background which is composed entirely of parts of the circuit which are operating satisfactorily in saturation conditions, albeit below the normal supply voltage. This reduces the possibility of circuit weak spots degrading the sensitivity of the tests.

The experimental set-up used for the comparison of search formats (see Fig.25) was described in Section 3.4. In the case of the binary search format, redundant illumination patterns were used to check that no combinational effects, due to illumination of large areas of the circuit, were present. The element of the 4 x 4 matrix responsible for the output error was found to coincide with the weak spot located using the SEM (which is limited to the spot scan mode) in the previous section. The defective area located using voltage contrast is in the adjacent element of the 4 x 4 matrix (see Fig.36). The marginal voltage shift under illumination conditions was a few mV whereas the electron beam produced a shift of the order of 100 mV.

Whereas no hysteresis effects were observed for simple bipolar gates, there was pronounced hysteresis for the TTL comparator. When the supply voltage was decreased to 4.25 V the logic error was detected and correct operation was not resumed until the supply voltage was increased to 4.65 V.

6 COMBINED SCANNING OPTICAL AND SCANNING ELECTRON MICROSCOPY

6.1 The Hybrid Solution

The use of the SEM in the voltage contrast mode in combination with an automated circuit tester is well known, as are the problems of beam damage effects in MOS devices, and, to a lesser extent, bipolar devices. Similarly, the SEM has been used in combination with the marginal voltage technique to highlight areas associated with an anomalous marginal voltage, and to superimpose such images on the normal secondary electron image. Previous work, at British Telecom, has concentrated mainly on bipolar devices, although a scanning light spot system has been demonstrated for both bipolar and MOS devices in conjunction with marginal voltage analysis. This system, which incorporates mechanically-stepped mirror drives, allows the interrogation of a 32 x 32 matrix of positions on the device under test - which is equivalent to a resolution worse than 100 microns on a 5 mm square chip, although the resolution improves in inverse proportion to the field of view. A conventional optical microscope is used to register the scanning light spot with a reflected light image of the DUT. Table 1 shows that with a X10 objective the SOMSEM resolution is better than four microns with an 8 mm field of view, with the additional advantage of automatic registration with an OBIC image. We conclude that provided the intensity available in the SOMSEM is sufficient to induce significant marginal voltage shifts (which is certainly the case for simple CMOS devices - see 5.4 below) there are significant advantages, particularly since the same instrumentation allows both bipolar and MOS testing (using electron beam stimulation and optical stimulation respectively) without duplication of expensive circuit testing facilities. Furthermore, using long-persistence phosphors coupled with programmable beam blanking would allow search formats other than the simple raster pattern. When a defective area is located, the various imaging modes of the SEM may be used as in conventional failure analysis.

6.2 The ERA SOMSEM

The optical stimulation of semiconductor devices in the SEM has been achieved by converting the scanning electron beam into a scanning optical beam using a phosphor screen and lens system as shown in Fig.41. The specimen current amplifier of the SEM may be used to obtain an OBIC image of the device-under-test using the video processing unit and any digital image processing facility attached to the SEM. The attainable resolution is limited by:

(i) phosphor grain size effects - the speckle apparent on OBIC micrographs is due to the inhomogeneity of cathodoluminescent efficiency as the electron beam traverses individual grains and their boundaries. Although the phosphor grain size is typically of the order of 3-6 microns, the projected optical raster is a demagnified version of the electron beam raster (e.g. in the ratio of approximately 3:1 for a X10 microscope objective depending on the working distance) and thus the speckle is of the order of one or two microns.

(ii) diffraction-limited spot size - this depends on the aperture of the imaging lens according to the Rayleigh Criterion.

(iii) charge spreading effects - similar, but not identical to those associated with the electron beam generation volume coupled with charge carrier diffusion effects when using the SEM EBIC mode.

(iv) reflections and multiple reflections - associated with refractive index changes e.g. at oxide layer interfaces.

(v) signal-to-noise ratio in the image - as for normal SEM micrographs, resolution depends on intensity of stimulation which in turn depends on the SEM operating conditions (chosen to avoid phosphor degradation), the phosphor efficiency, and the f/No. of the optical system.

Using the optical projection system shown in Fig.42 together with the constraint that the total working distance from phosphor screen to specimen does not exceed 8 cm, the resolution of various standard microscope objectives has been assesed together with their field of view and effective magnification. The results obtained with the USAF resolution test target (see Fig.43) are shown in Table 1. The normal working distance of microscope objectives is considerably longer, and spherical and chromatic aberrations are corrected for a tube length of 16 cm. Consequently one would not expect optimum performance for conventional microscope objectives when used at magnifications well below their stated design. However, as Table 1 shows, the resolution attainable is of the order of one to four microns, and other factors such as phosphor grain size and focussing errors will often be more of a limitation than the minimum spot size.

6.3 OBIC Images

The formation of OBIC images using the SOMSEM is analagous to the EBIC mode of the SEM. However, the beam induced currents are several orders of magnitude lower, mostly because of losses due to the collection efficiency of the optical system, but also due to the low efficiency of the phosphor screen itself (~10%). It

is necessary to operate the SEM with maximum beam current consistent with minimum phosphor degradation, and for the Cambridge Stereoscan 250 at 20 kV the largest objective aperture was selected with 'spot size 4' (corresponding to an electron probe size of ½ micron).

The resolution of the OBIC images, already adequate for many purposes, could be improved with better optical design and luminescent single crystal screens to eliminate phosphor grain size effects. Levy et al (Ref.9) have proposed a semiconductor laser double heterostructure screen which emits light when pumped by an electron beam. Since the emitted light is more directional than for a phosphor, the overall efficiency should be greater, and such a development would combine the high-intensity advantage of laser-based scanning optical microscopes with the inertialess, highly versatile scanning already inherent in the SOMSEM. In the context of resolution, it should be emphasised that the resolution of the EBIC mode of the SEM is seldom better than one micron, being limited by the beam generation volume coupled with charge spreading effects. In fact, Wilson et al (Ref.10) have shown that the resolution of the scanning optical microscope may be identical for certain applications, such as the imaging of electrical effects associated with dislocations in optoelectronic materials.

During the present contract, the quality of the SOMSEM images has improved steadily, although it has not been possible to combine the best images with marginal voltage investigations because of the additional noise introduced by the latter.

Although the use of the EBIC mode for the imaging of MOS devices is totally unsuitable for non-destructive failure analysis, it is nevertheless interesting to compare OBIC and EBIC images, and also conventional reflected light images. A series of low and high magnification images are shown in Figs.44, 45 and 46 using conventional optical microscopy, the EBIC and OBIC modes respectively. Conventional optical microscopy (Fig.44) tells us little about the electrical properties of the device in any direct sense, although failure analysts frequently use the optical microscope (often after electrical testing) in combination with sectioning techniques, to locate shorted junctions or migration of the aluminium metallisation, for example. The well-known EBIC technique is illustrated in Fig.45, and it is clear that sub-surface information is obtained regarding the electrical behaviour of junctions. Electron-hole pairs generated by the beam of the SEM

move under the influence of electric field whether externally applied or arising from dopant profiles. For example in the vicinity of pn junctions, the electron-hole pairs will be separated giving rise to an induced voltage or induced current. Although the mechanism for image formation in the OBIC mode is almost identical, Fig.46 demonstrates that deeper junctions may be observed compared with EBIC. In the present case, this is not because the photons penetrate the silicon more than the 20 keV electrons used to produce Fig.45, but rather that the electrons penetrate the passivation layer much less readily than light.

The present resolution of the SOMSEM (between one and two microns for the X40 objective) is sufficient for many failure analysis purposes, especially when the OBIC mode is considered as a non-destructive technique prior to the more detailed, but destructive, imaging modes of the SEM. Furthermore, due to the compatibility with the existing instrumentation of the SEM, the ease of use and range of magnifications available with the SOMSEM is unsurpassed by any other scanning optical microscope, even though its ultimate resolution is not quite as good as the best laser-based system.

6.4 Marginal Voltage Studies with the SOMSEM

Additional leadthroughs to the vacuum chamber of the SEM were required for marginal voltage studies using the SOMSEM in order to control the input words and monitor outputs whilst varying the supply voltage. The principal objectives were to confirm that sufficient intensity is available to induce realistic marginal voltage changes and that such changes are compatible with, and could be superimposed upon, OBIC images.

It has previously been shown (Section 3) that increasing intensity increases the marginal voltage for logic level '0' outputs for all CMOS gates when measured under virtually open-circuit conditions. For logic level '1' outputs, the marginal voltage shift may be positive or negative depending on the gate type, and this shift is observed for both low (greater than 1 MΩ) and high impedance measurements. We have demonstrated, using the procedures outlined below, that the intensity presently available within the SOMSEM (50-100 $\mu W/cm^2$ for the X10 objective and greater for the X40 objective) is sufficient to induce easily-measurable marginal voltage shifts of about 100 mV for both low and high gate outputs. Typical operating conditions of the Cambridge S250 were:

electron beam voltage 20 kV
spot size 4 (electron probe size $\frac{1}{4}$ μ), aperture 50 μ
beam current 10^{-7} A

A Keithley model 601 electrometer was used to monitor gate 'low' outputs as the device was slowly optically scanned for different values of supply voltage. For supply voltages more than 0.1 V below the marginal voltage, the nominal gate 'low' outputs rose to the supply voltage when stimulated with the scanning light beam. Above the marginal voltage, the outputs remained at zero.

Gate high outputs may easily be connected to the specimen current amplifier through a 1 MΩ series resistor to obtain a logic state map. Logic level changes of 1 V then register as current changes of 1 μA. With the device held at the marginal voltage for a particular input word, these changes occur when the scanning light spot illuminates the part of the device responsible for the corresponding logic output. The logic level image obtained on the SEM monitor was superimposed on an OBIC image (using double exposure - see Fig.47). The bright area corresponds to the logic level change and it is indeed associated with the particular gate being addressed by the input word. Fig.48 shows another device imaged in the OBIC mode and Fig.49 shows the same device with the output of one of the four gates superimposed. There is some misorientation of the images because of a specimen movement between the two exposures - the stage was withdrawn from the SEM to change the input connection to the SCA. Figures 50, 51 and 52 show how the logic output image changes as the function of supply voltage in the vicinity of the marginal voltage for 100 mV steps.

The images are not of the same quality as the OBIC images we have reported previously (Ref.4) because of phosphor deterioration (mainly due to handling) and noise/pick-up introduced into the system as a result of the additional wiring and the various power supplies. These problems could be avoided in a properly engineered system. Furthermore, the effect of possible specimen movement during the double exposure technique could be circumvented by electronic addition of the OBIC and logic information signals. However, it is clear that there is sufficient intensity to induce realistic marginal voltage shifts.

In an automated testing context, comparator circuitry would normally be used to compare the DUT with a known good reference device. The output of the

comparator circuitry is then connected to the video processing instrumentation of the SEM through the specimen current amplifier as before.

The outputs of a 4-dual input NAND gate MOS device were compared with those of a known good reference device using the circuit shown in Fig.53. If the logic outputs are the same (according to the definitions in Section 2.3), then the output of the comparator is zero, (PASS). If the logic outputs are different, then the output of the comparator circuitry is 1, (FAIL). The supply voltage to the device-under-test is progressively lowered until a FAIL condition is indicated - see for example Fig.54. If the DUT is illuminated, then the PASS condition may be re-established, corresponding to the decrease in marginal voltage. If there is an increase in marginal voltage on illumination then clearly the supply voltage to the DUT must be set first above the FAIL threshold level, and the comparator output will change from PASS to FAIL when the device is illuminated. The comparator output was inverted using a CMOS inverter before connecting to the SCA through a 1 MΩ resistor - this is because SCAs of SEMs are normally designed to amplify negative conventional currents. The results of such experiments are shown in Figs.55, 56 and 57, and illustrate the location of areas associated with particular input words and their corresponding marginal voltages. Fig.58 shows the OBIC image of the device at the same magnification. For normal devices, these areas correspond to circuit 'weak spots', a concept developed in Section 5. In the case of defective devices the location of specific defects should be considerably easier, provided anomalously high marginal voltages are associated with the defects. This is because for an anomalously high marginal voltage, parts of the device other than the defective area should be well away from marginal operation.

7 EXTENSION TO SEQUENTIAL CIRCUITS

7.1 Introduction

A sequential circuit differs from a combinational circuit in that at any instant in time its output depends not only on the input word but also on previous words. In a sense a sequential circuit may be regarded as a combinational circuit with a capacity for storing binary information and also an additional input word - the clock pulse.

Depending on the precise moment of reduction of the supply voltage relative to the clock pulse, workers at British Telecom proposed different definitions of marginal voltage for a particular word in a sequence of output words. The definitions of 'permanent', 'dynamic' and 'immediate' marginal voltage are given in Ref.6, but it is not necessary to distinguish between them to explore the validity of different search formats for sequential circuits. Suffice to say that for combinational circuits 'immediate' marginal voltage is the only relevant measurement, and for the purposes of extending the study to sequential circuits, it is this definition we have in mind.

The measurement of immediate marginal voltage proceeds as follows. A test sequence of words are monitored. If, during the application of a particular input word (say the nth word), the supply voltage is reduced from its normal value which just corrupts the output data, then the critical value of supply voltage is termed the immediate marginal voltage for that particular input word. The procedure is repeated for the (n + 1)th word and so on, but each time the circuit is reset before applying the test sequence. Clearly this is time-consuming but nevertheless inevitable.

7.2 Search Formats for Sequential Circuits

When anomalous marginal voltages are detected in sequential circuits, it is particularly desirable to locate their origin in the circuit before conventional failure analysis, because of the increased complexity, compared with combinational circuits. However, interrogation of the circuit at each of, say, 10^6 positions in a 1000 x 1000 matrix would be totally out of the question during what is already an extended electrical test. British Telecom have, however, demonstrated the

technique for a 32 x 32 matrix using the raster or spot scan mode. The binary search technique which we have demonstrated is clearly much more desirable especially if higher resolution is required.

During their investigations using the spot scan, workers at British Telecom showed that areas surrounding defect may correspond to both positive and negative marginal voltage shifts. It can be argued that the simultaneous stimulation of these areas during the binary search format (and, to a lesser extent, the strip search format) may greatly reduce the magnitude of the marginal voltage shift thus making defect location impossible. However, we have shown experimentally that, for combinational circuits at least, defect location is possible using search formats more efficient than the spot scan. We postulate that the exact cancelling of the positive and negative contributions to the marginal voltage shift is most unlikely, and if this did occur for a particular defect the solution is to use the less efficient, more localised search formats. Even in the case of the spot scan mode, the potential cancellation problem is not entirely eliminated, unless the size of the stimulating spot is less than the area containing both positive and negative contributions. If the spot is too small, however, there will be insufficient stimulation to induce a logic error, and the number of spot positions will be enormous with a corresponding increase in testing time.

We therefore conclude that the same problems are inherent in all three different search formats, to a greater or lesser degree, without prior knowledge of the extent of the defective area. If there is insufficient sensitivity for a particular investigation with the more efficient search formats, then the spot scan with variable spot size is the fall-back technique. Our experimental studies have shown no difference in sensitivity for the different search formats, but this is probably because the stimulated areas were very much larger than an individual transistor even in the spot scan mode. This is not, of course, a function of the optical design of the equipment, but rather a result of using the simple 4 x 4 matrix patterns to illustrate the basic principles. These principles are thought to be equally valid for sequential circuits, but there may be additional problems associated with hysteresis effects.

8 CONCLUSIONS

Despite the many variations encountered in the marginal voltage characteristics of simple gates, we have demonstrated that circuit weak spots may be successfully located using external stimulation with the circuit under marginal voltage conditions. Furthermore, the efficiency of the location procedure is greatly enhanced if more sophisticated search formats, such as the binary search, are used.

A new hybrid instrument, the SOMSEM, allows electron-beam stimulation of bipolar devices and optical stimulation of MOS devices within the same instrumentation. The light intensity presently available in the SOMSEM is sufficient to induce realistic marginal voltage changes in simple gates, but it is probable that higher intensities are required for more complex devices. Thus further development of the SOMSEM is necessary, for example, incorporating the laser heterostructure screen developed at Bell Laboratories. The resolution and field of view of the SOMSEM, are, however, entirely adequate for locating defective gates in integrated circuits. Logic state maps, obtained under marginal voltage conditions, may be superimposed on OBIC images to give the location of circuit weak spots.

The application of efficient search formats for locating defects in sequential circuits is an area of great potential, and simple high-intensity optical projection systems have a role to play here. Also, the characterisation of defects in integrated circuits using optical spectral response techniques has received insufficient attention in the past. Combining all these techniques with the SOMSEM system constitutes a powerful alternative to SEM voltage contrast techniques for routine inspection, especially since the influence of passivating layers is not of crucial importance. For failure analysis, voltage contrast and marginal voltage techniques should be treated as complementary, with marginal voltage analysis and binary search formats locating the defective area prior to voltage contrast examination.

The areas we would therefore recommend for further work are:

1. SOMSEM development for higher intensity.
2. Spectral response analysis of integrated circuits for process monitoring and failure analysis.
3. Comparison of search formats for sequential circuits to extend the procedures we have developed here.

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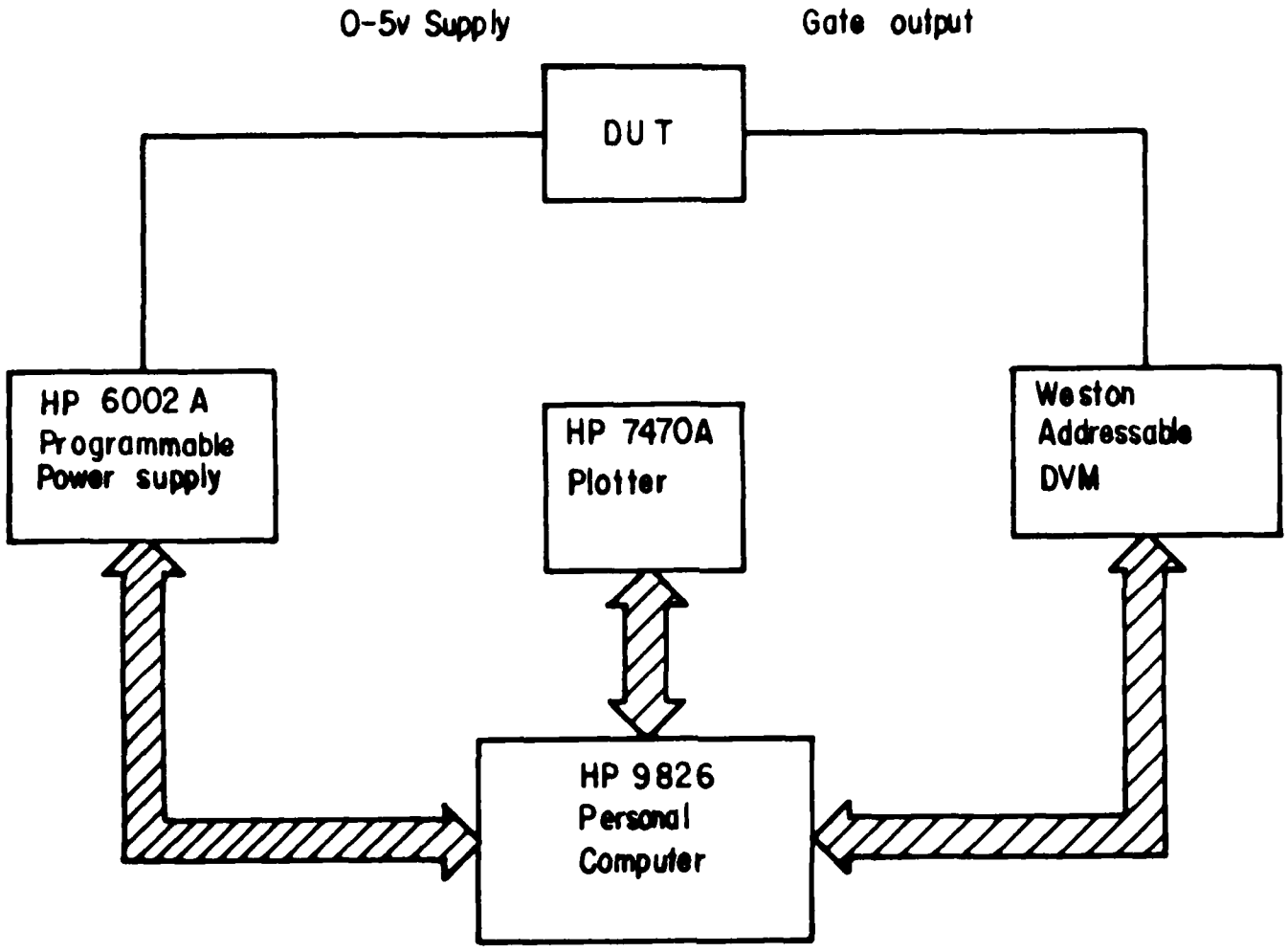


Fig.1: Marginal voltage characteristics measurement system

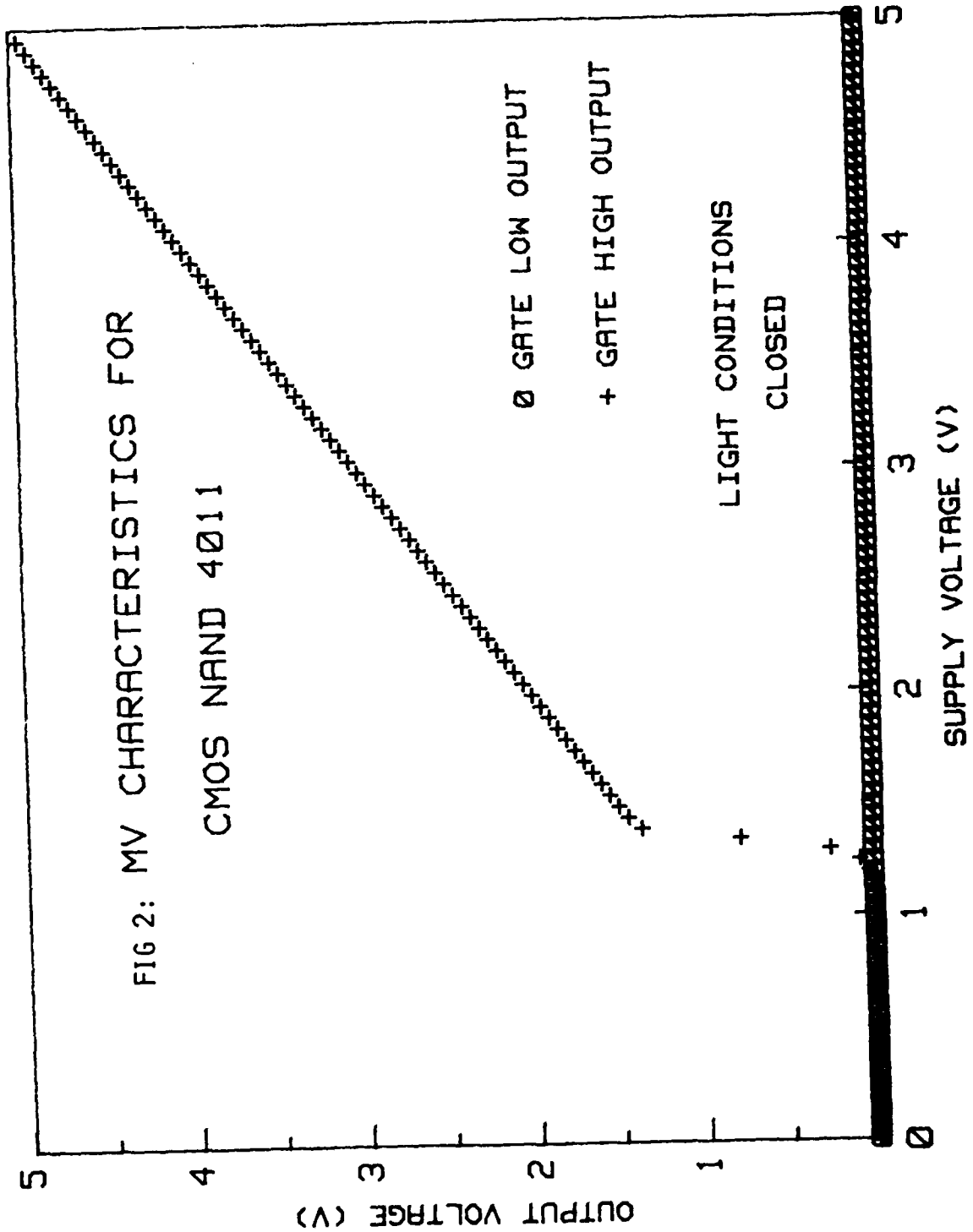


FIG 2: MV CHARACTERISTICS FOR
CMOS NAND 4011
Ø GATE LOW OUTPUT
+ GATE HIGH OUTPUT
LIGHT CONDITIONS
CLOSED
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
0
1
2
3
4
5

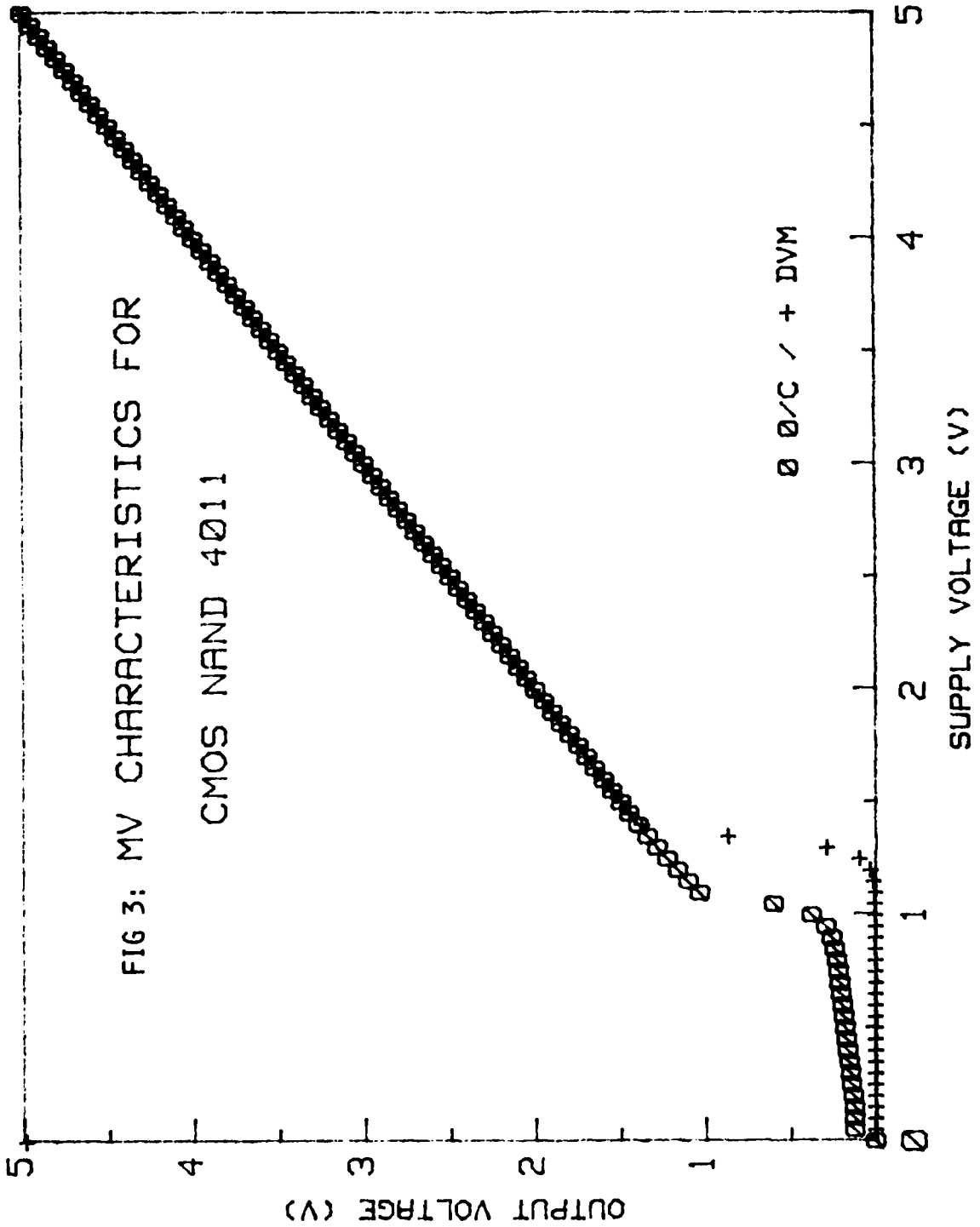


FIG 3: MV CHARACTERISTICS FOR
CMOS NAND 4011
Ø Ø/C / + DVM
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
0
1
2
3
4
5

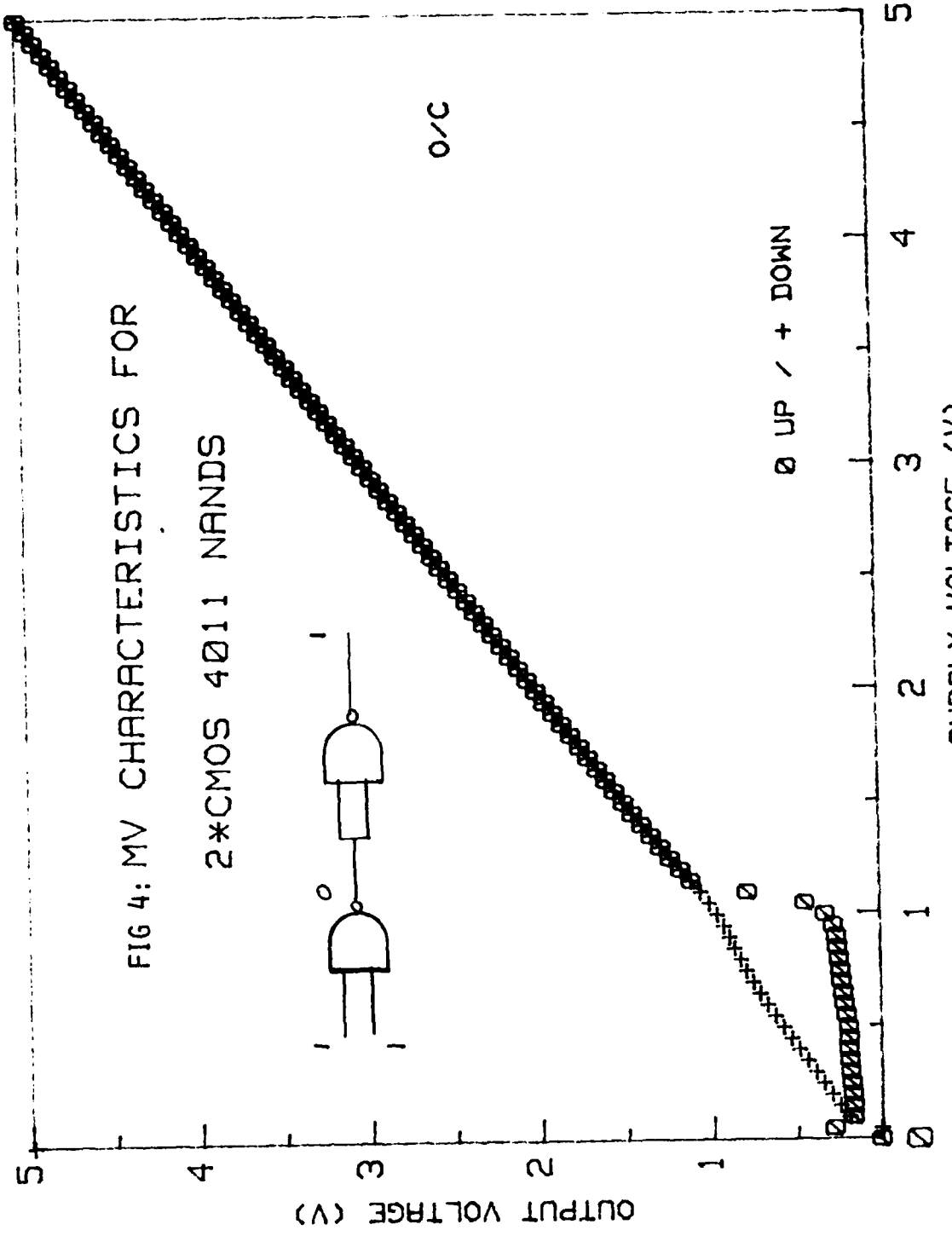


FIG 4: MV CHARACTERISTICS FOR
2*CMOS 4011 NANDS
0/C
Ø UP / + DOWN
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
0
1
2
3
4
5
I
O
I

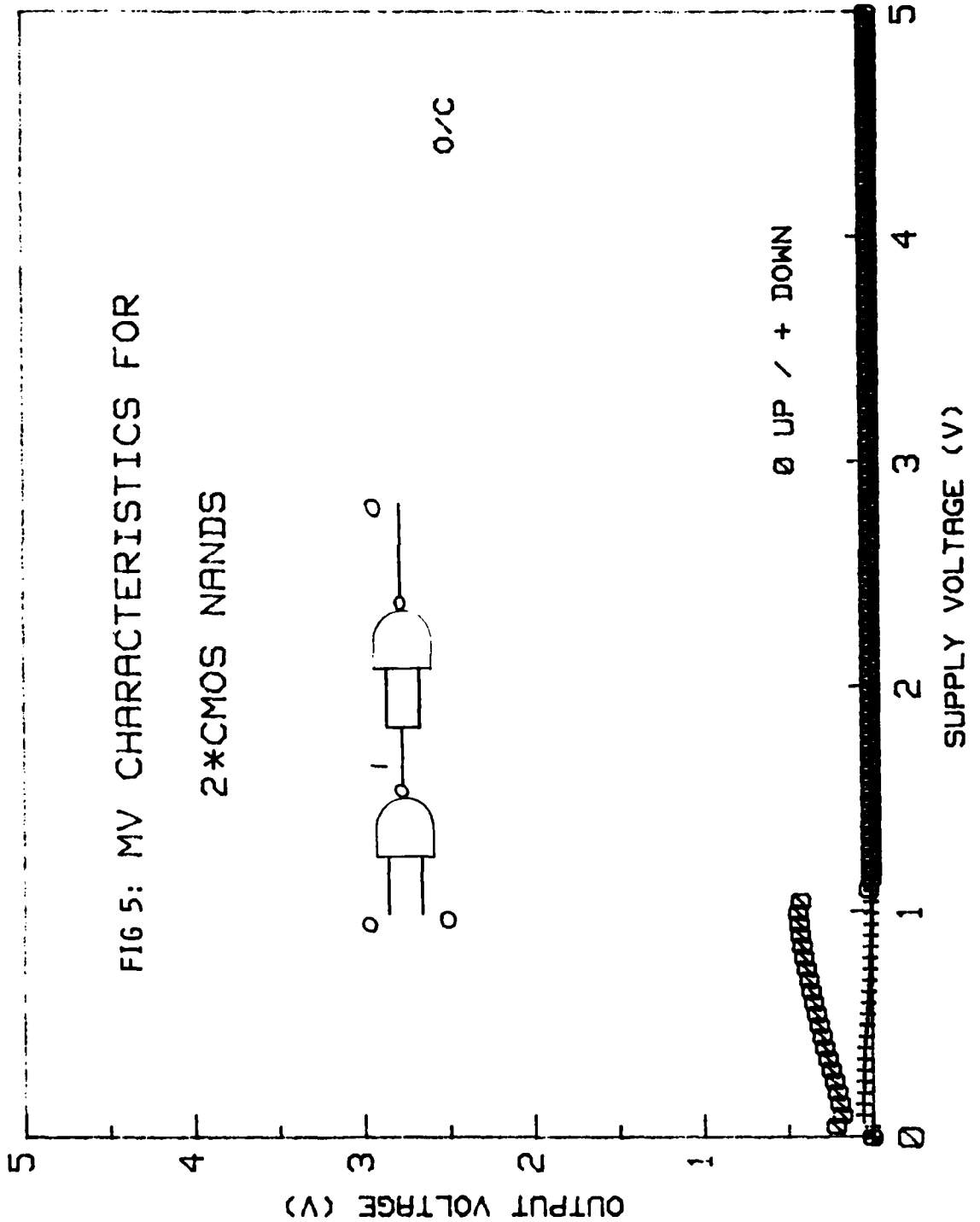


FIG 5: MV CHARACTERISTICS FOR
2*CMOS NANDS
O/C
Ø UP / + DOWN
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
0
1
2
3
4
5

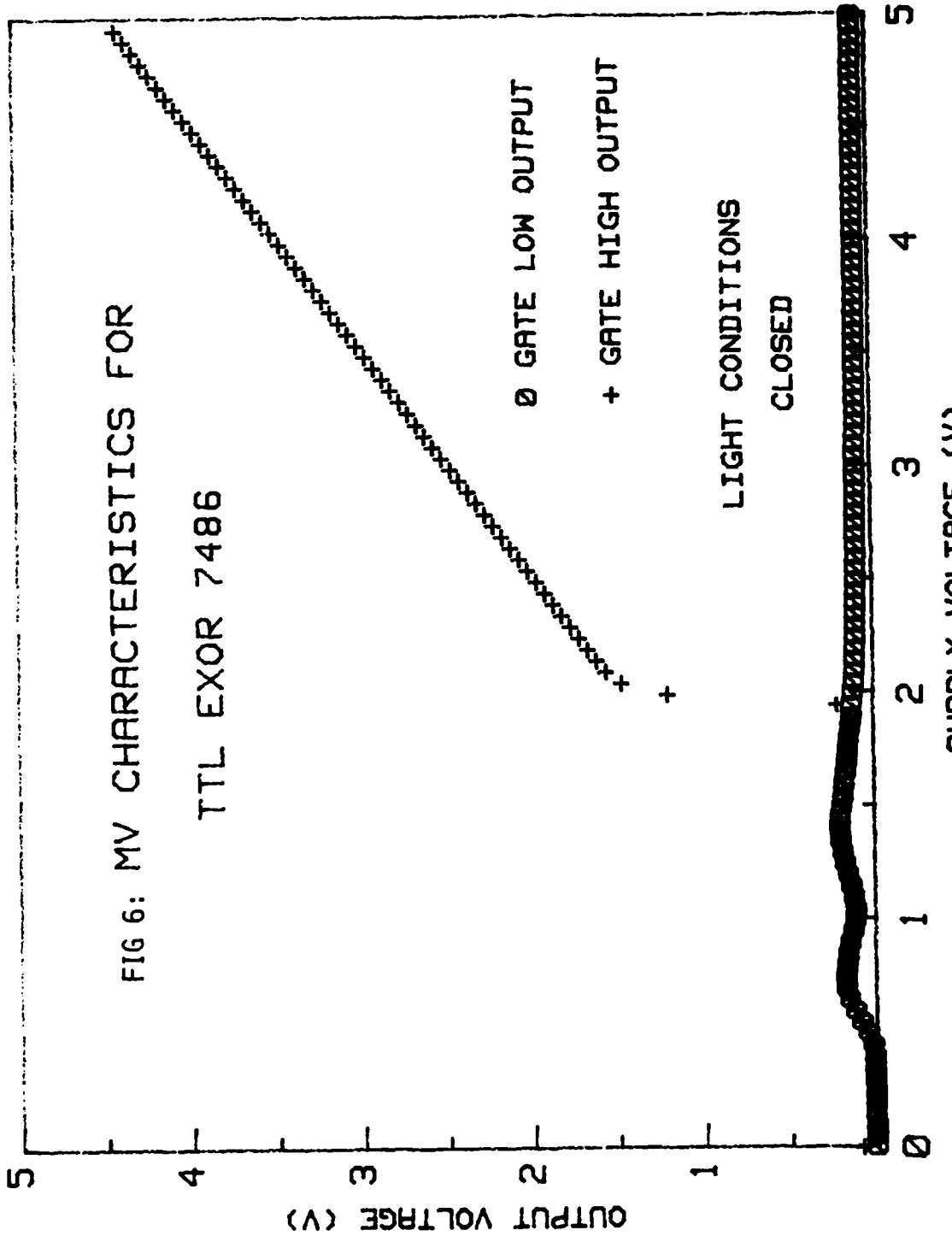


FIG 6: MV CHARACTERISTICS FOR
TTL EXOR 7486
Ø GATE LOW OUTPUT
+ GATE HIGH OUTPUT
LIGHT CONDITIONS
CLOSED
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
Ø
1
2
3
4
5

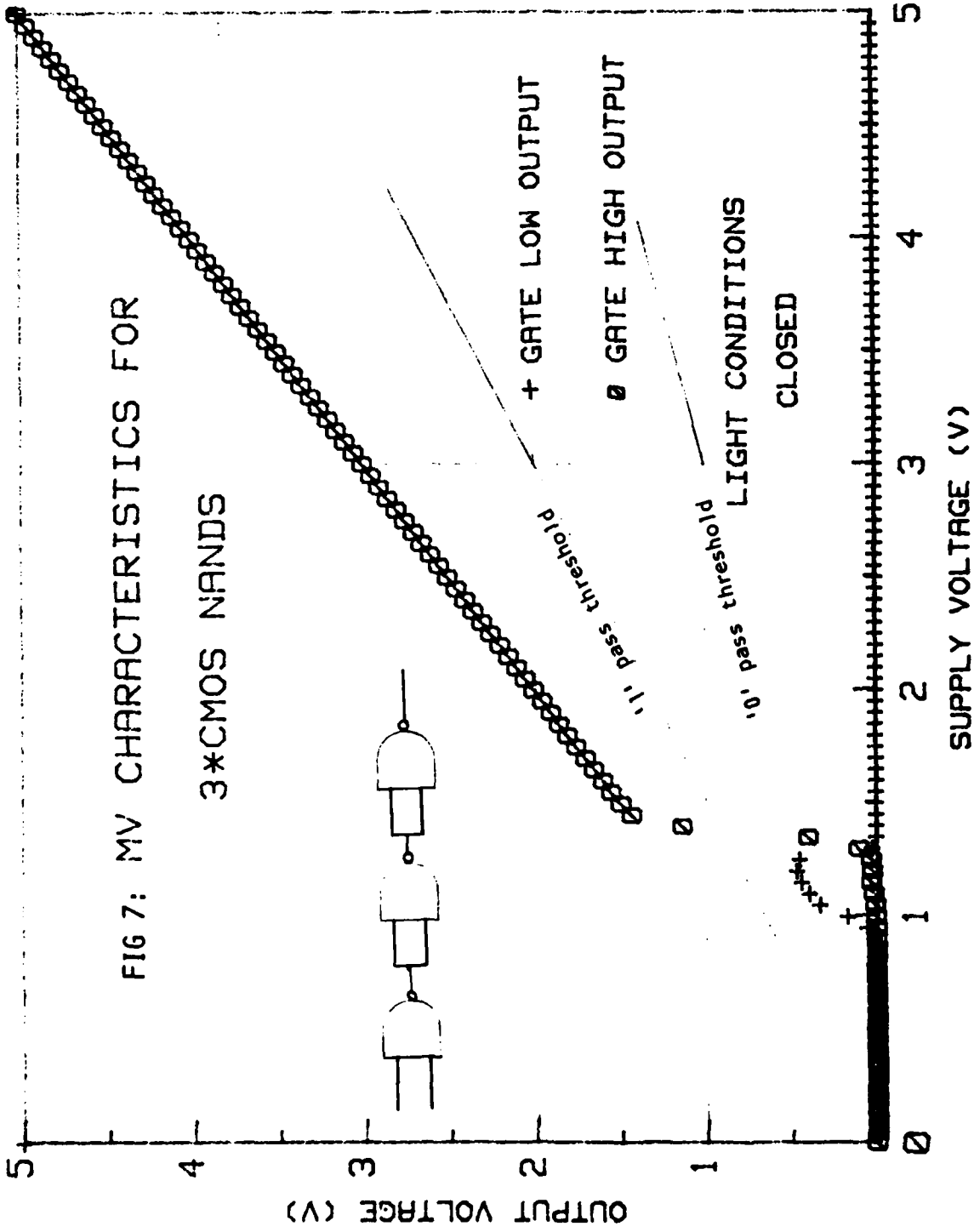


FIG 7: MV CHARACTERISTICS FOR
3*CMOS NANDS
+ GATE LOW OUTPUT
Ø GATE HIGH OUTPUT
'1' pass threshold
'0' pass threshold
LIGHT CONDITIONS
CLOSED
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
0
1
2
3
4
5

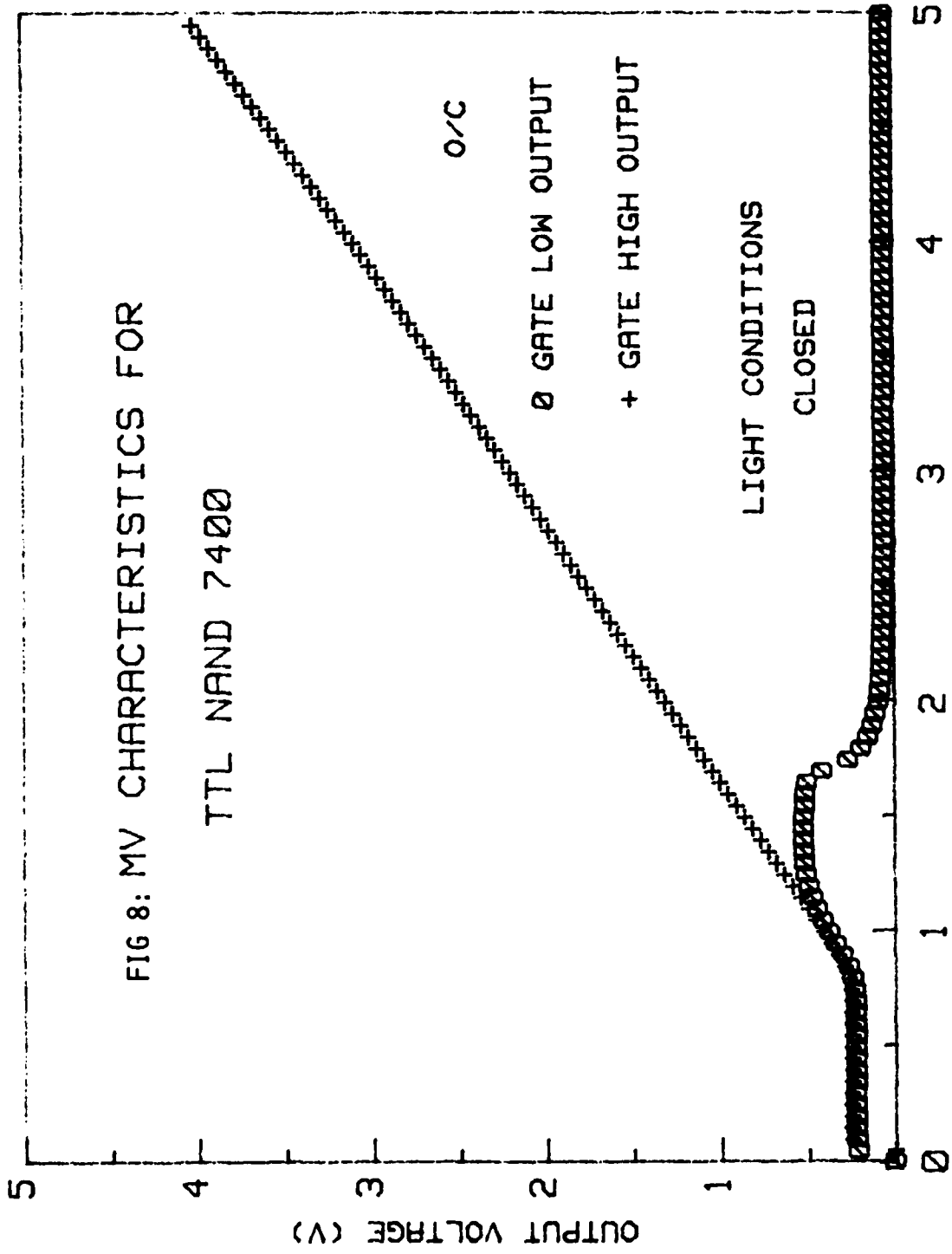


FIG 8: MV CHARACTERISTICS FOR
TTL NAND 7400
O/C
Ø GATE LOW OUTPUT
+ GATE HIGH OUTPUT
LIGHT CONDITIONS
CLOSED
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
0
1
2
3
4
5

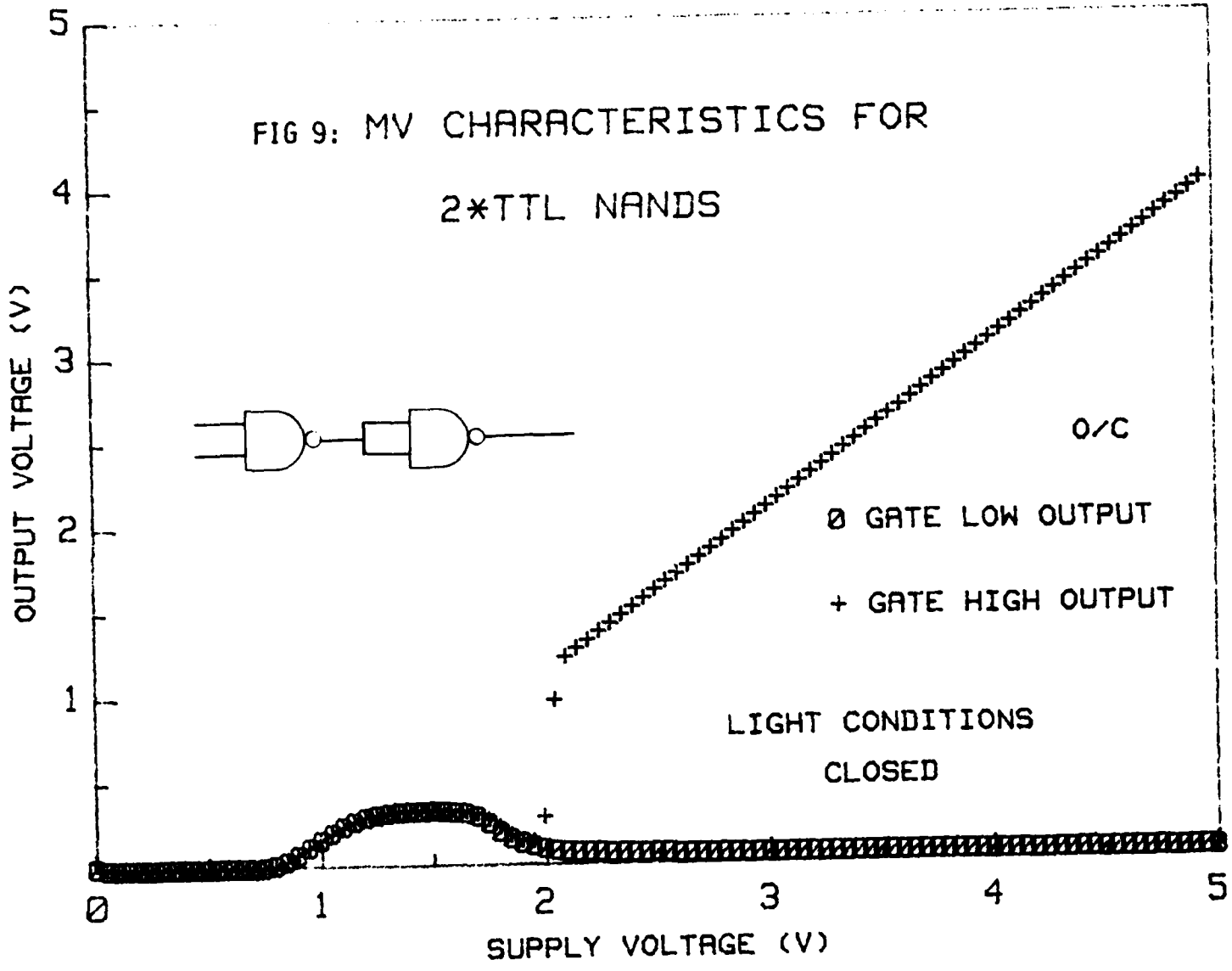


FIG 9: MV CHARACTERISTICS FOR
2*TTL NANDS
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
0
1
2
3
4
5
O/C
Ø GATE LOW OUTPUT
+ GATE HIGH OUTPUT
LIGHT CONDITIONS
CLOSED

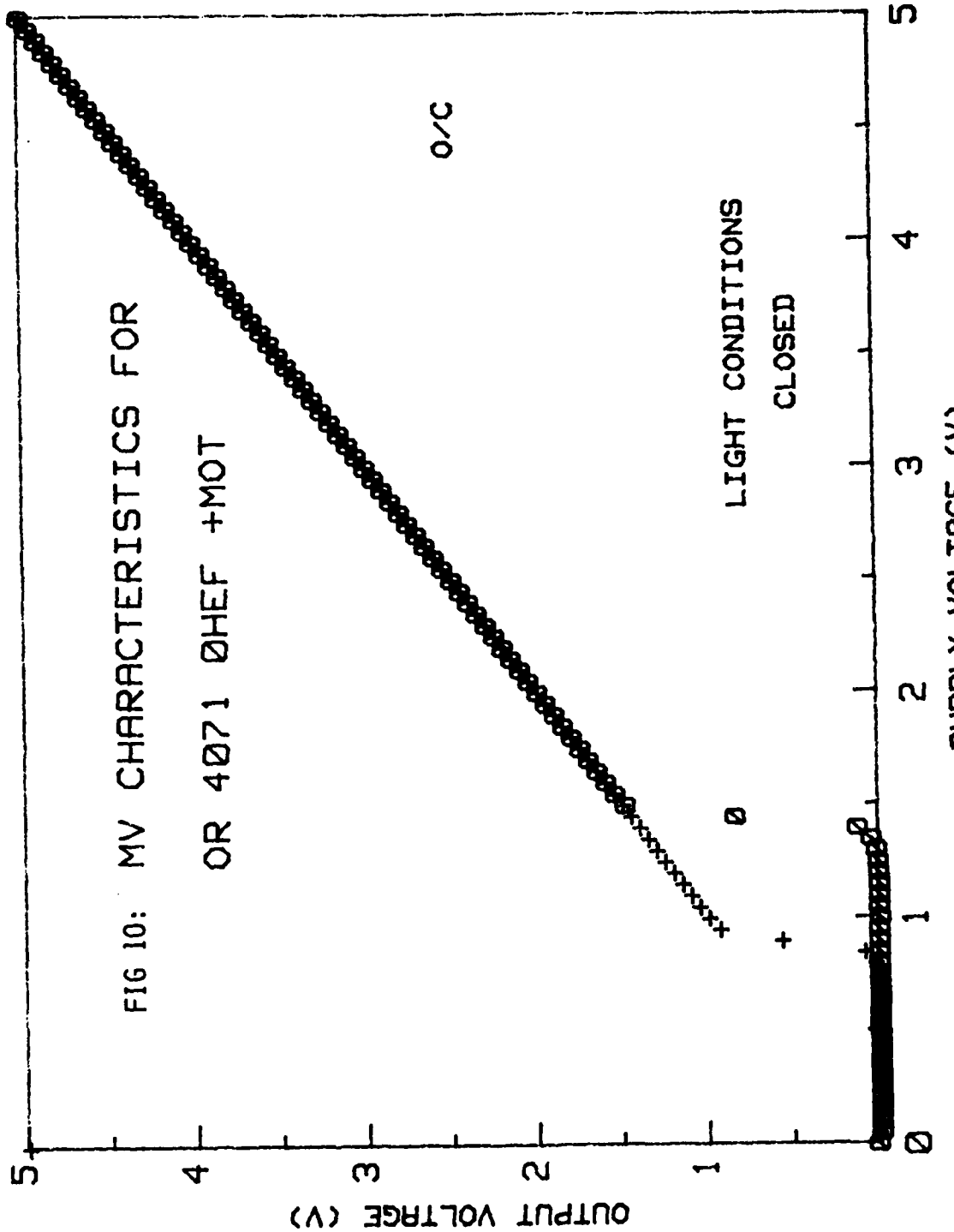


FIG 10: MV CHARACTERISTICS FOR
OR 4071 ØHEF +MOT
O/C
LIGHT CONDITIONS
CLOSED
Ø
+
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
0
1
2
3
4
5

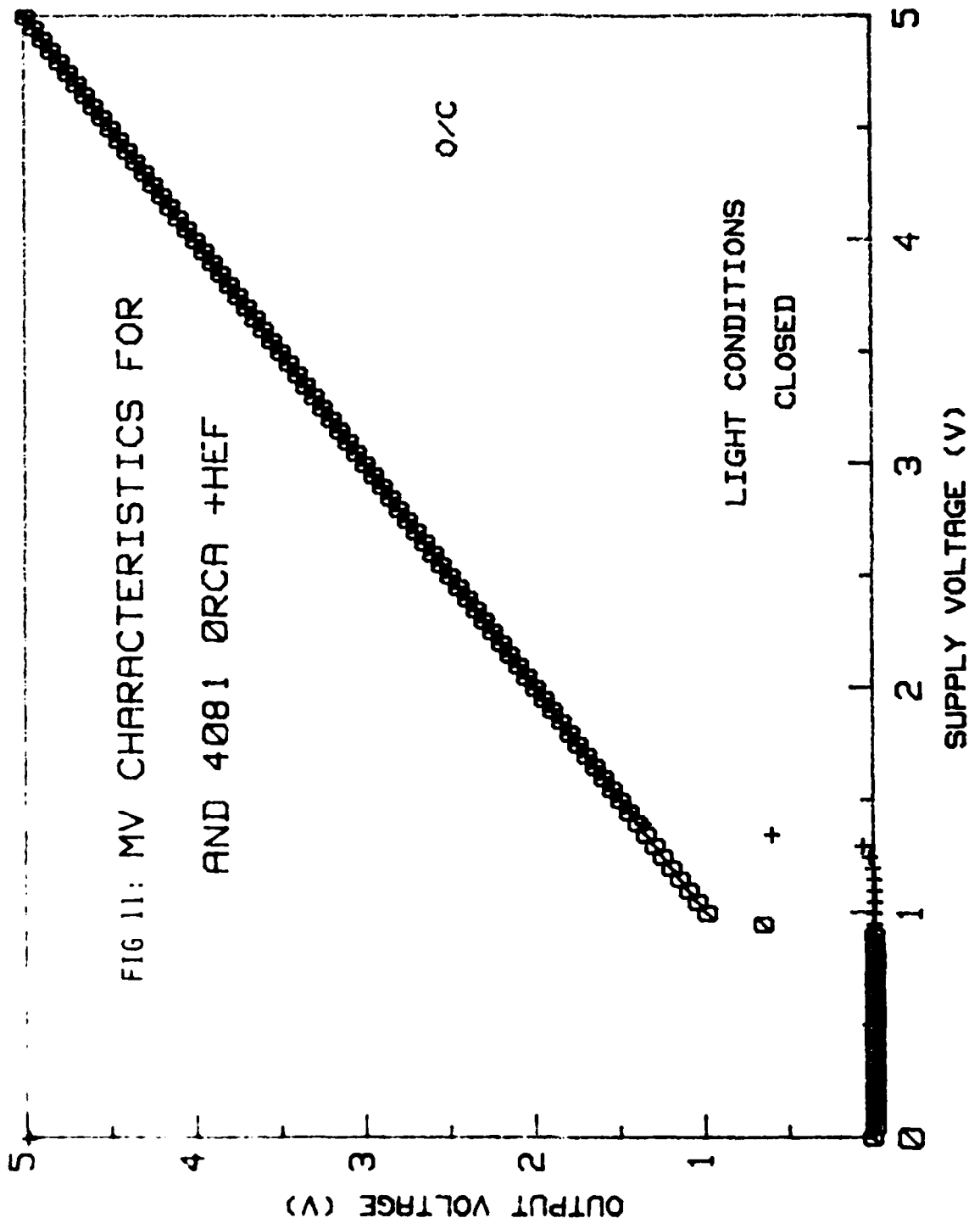


FIG 11: MV CHARACTERISTICS FOR
AND 4081 ØRCA +HEF
O/C
LIGHT CONDITIONS
CLOSED
Ø +
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
Ø
1
2
3
4
5

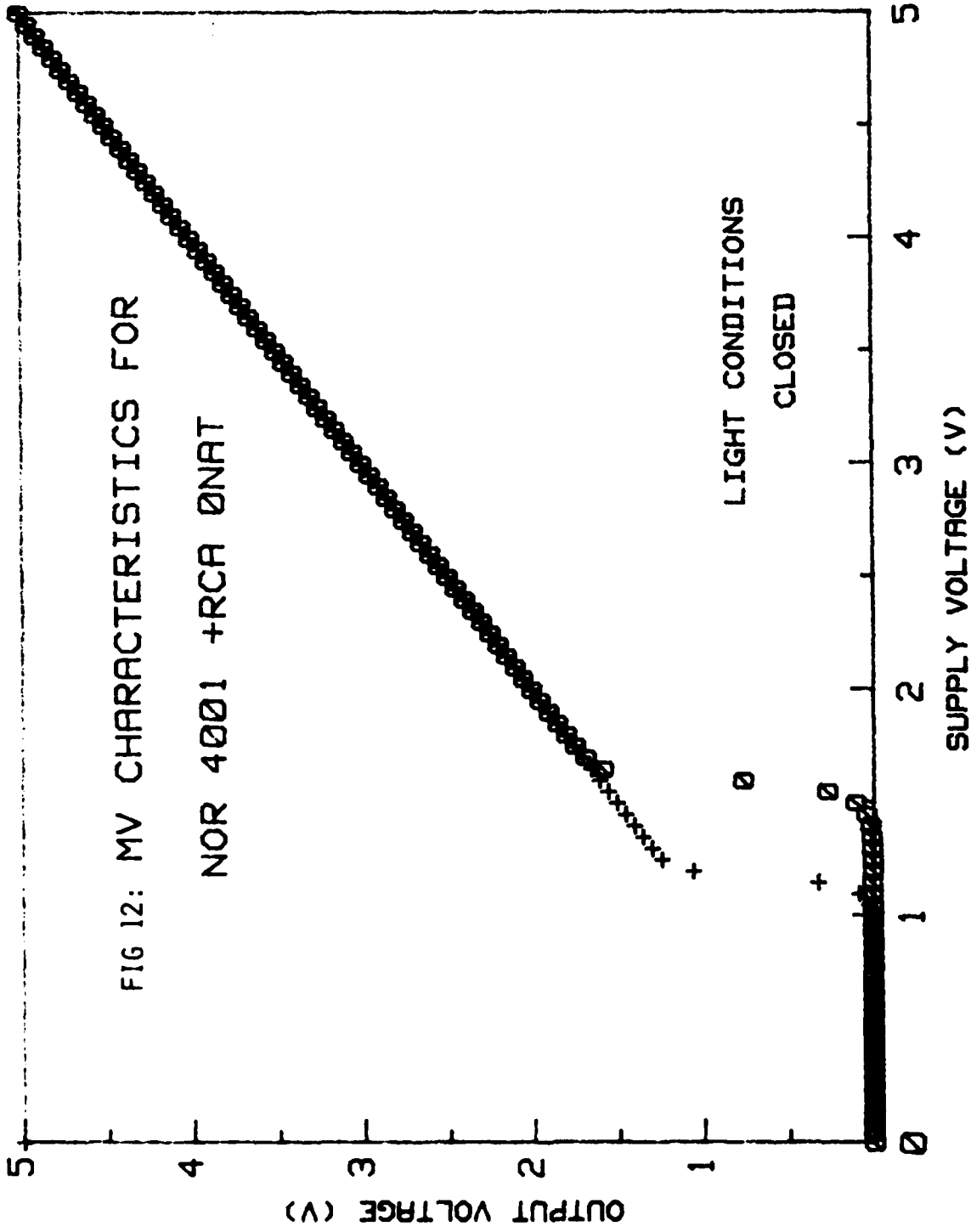


FIG 12: MV CHARACTERISTICS FOR
NOR 4001 +RCA ONAT
LIGHT CONDITIONS
CLOSED
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
0
1
2
3
4
5

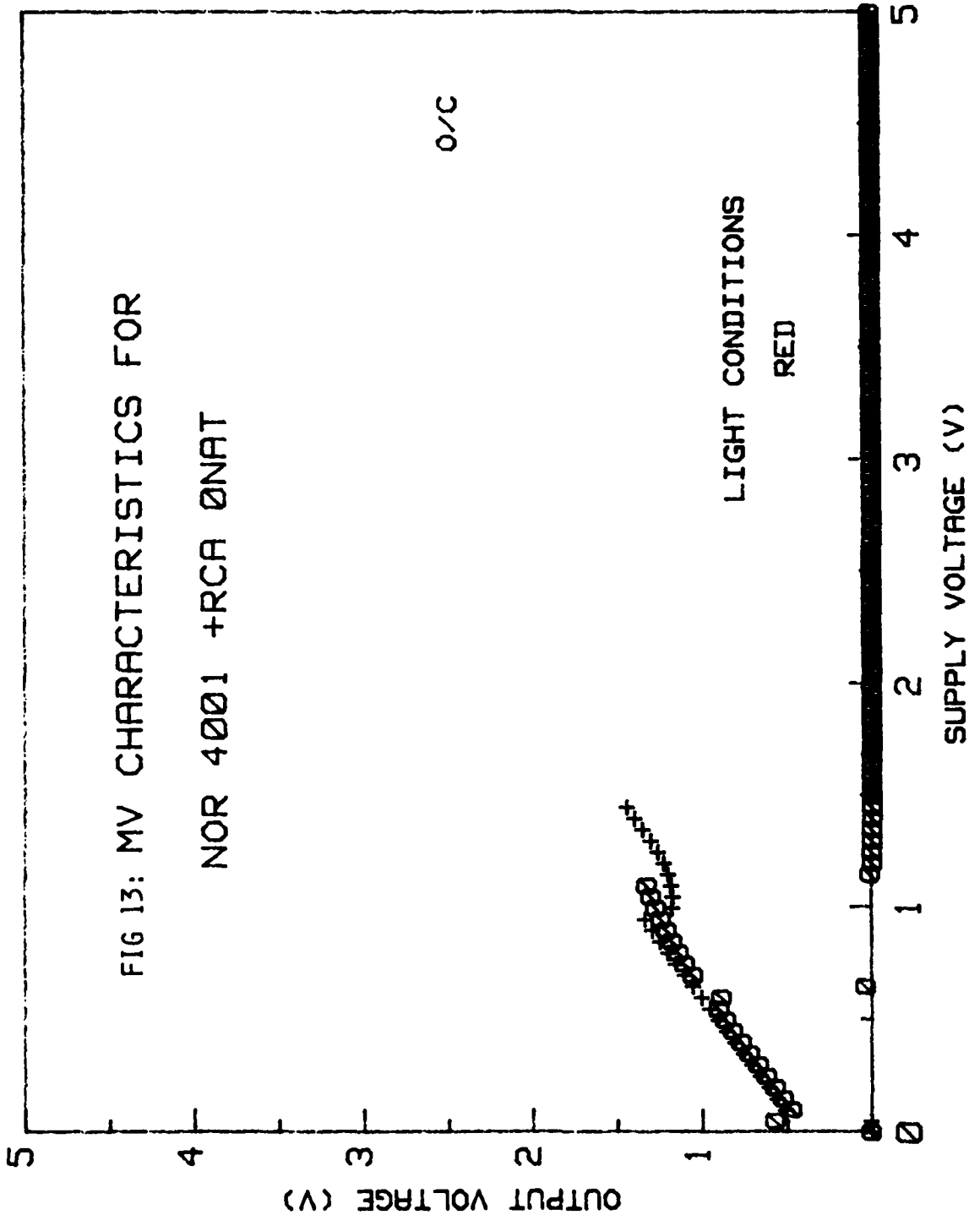


FIG 13: MV CHARACTERISTICS FOR
NOR 4001 +RCA ONAT
O/C
LIGHT CONDITIONS
RED
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
0
1
2
3
4
5

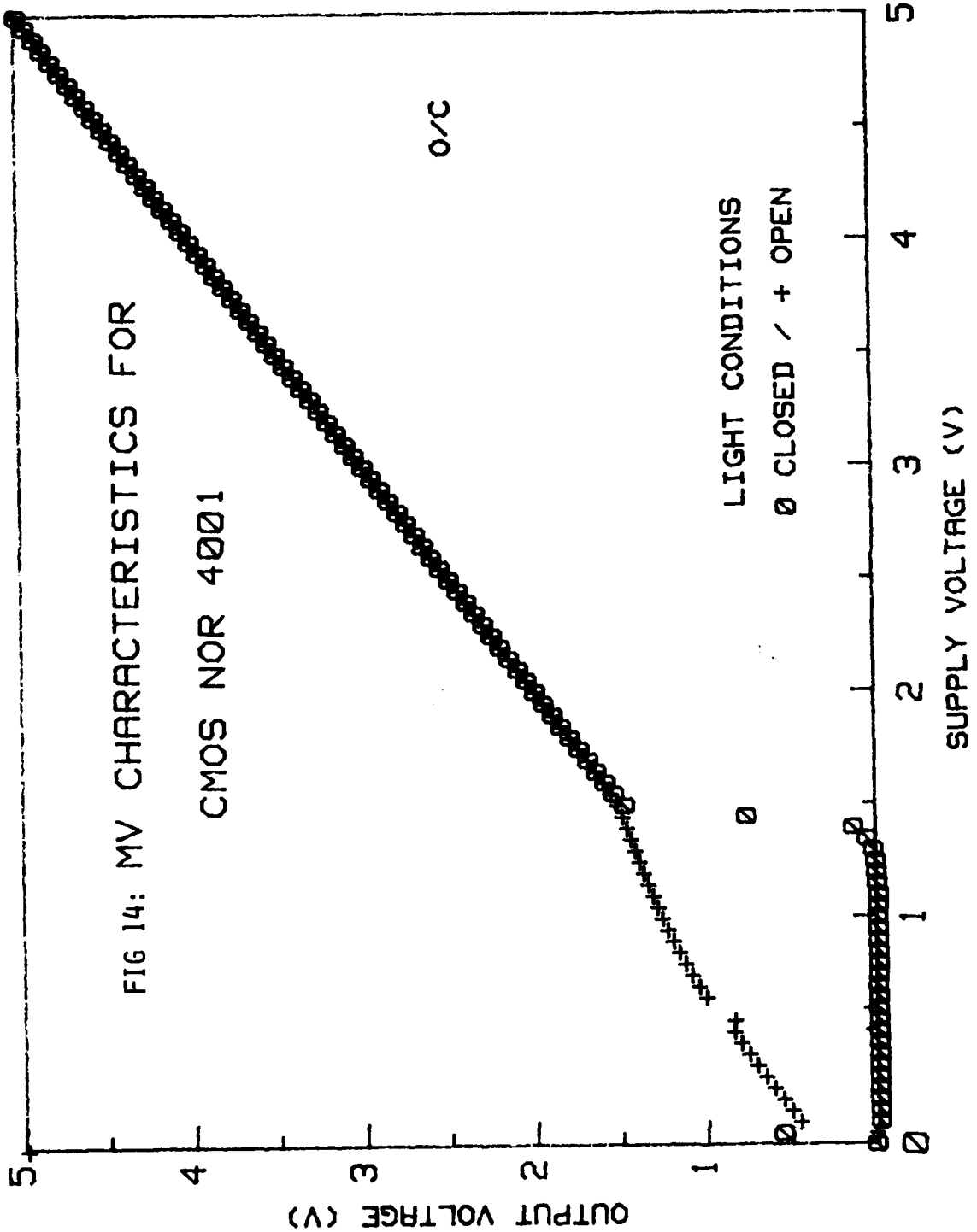


FIG 14: MV CHARACTERISTICS FOR
CMOS NOR 4001
O/C
LIGHT CONDITIONS
Ø CLOSED / + OPEN
Ø
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
0
1
2
3
4
5

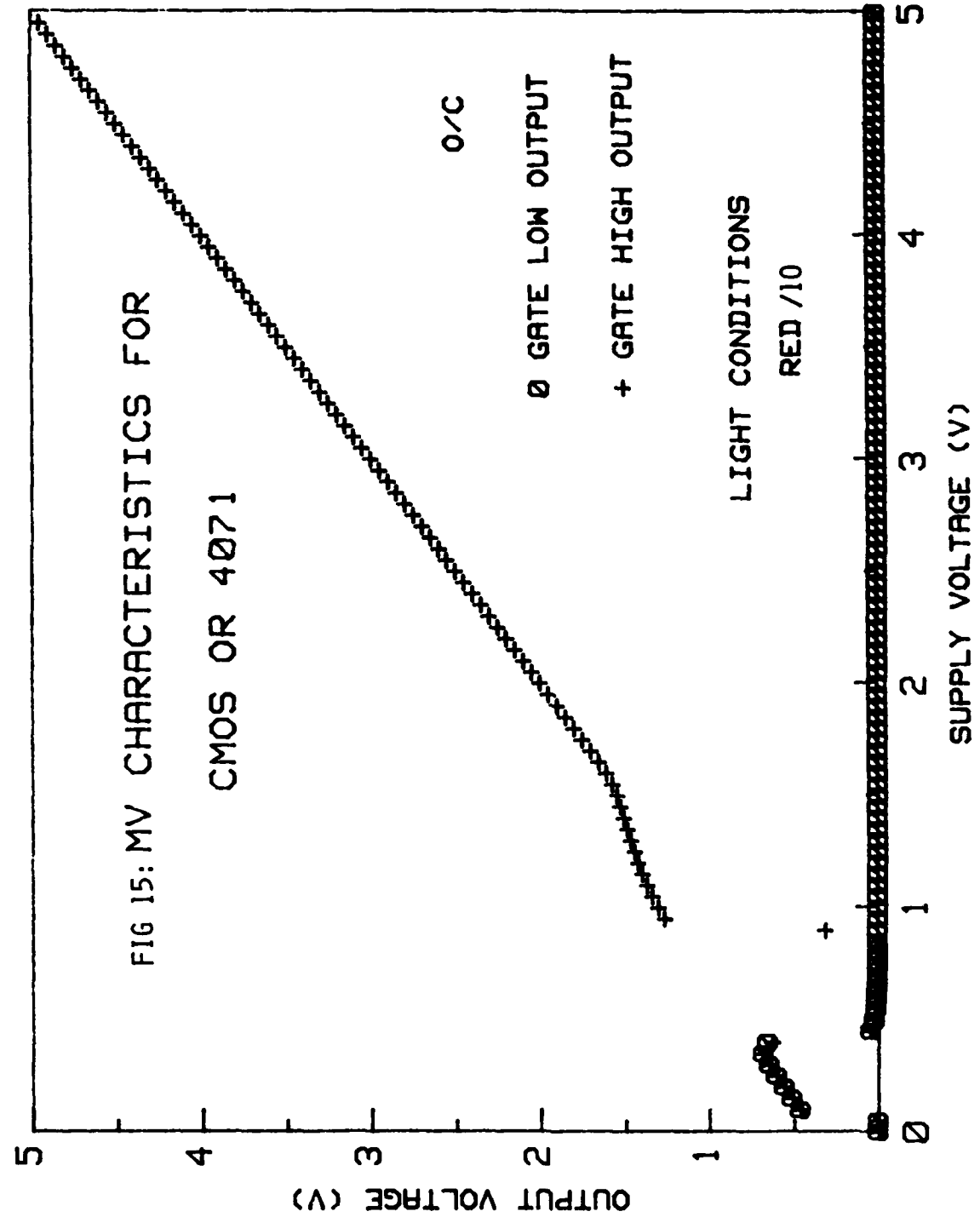


FIG 15: MV CHARACTERISTICS FOR
CMOS OR 4071
0/C
Ø GATE LOW OUTPUT
+ GATE HIGH OUTPUT
LIGHT CONDITIONS
RED /10
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
0
1
2
3
4
5

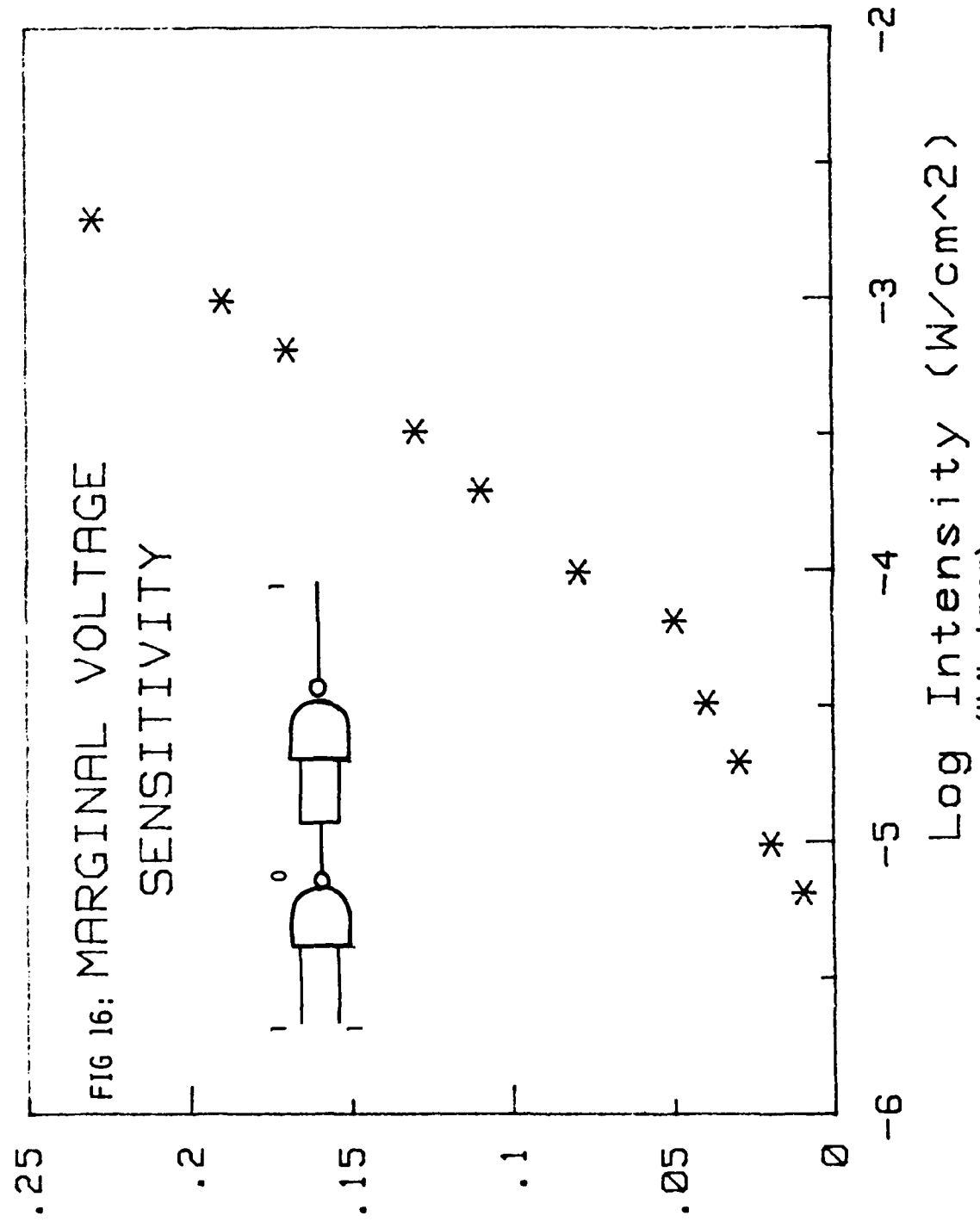


FIG 16: MARGINAL VOLTAGE
SENSITIVITY
Marginal Voltage Shift (V)
.25
.2
.15
.1
.05
0
-6
-5
-4
-3
-2
Log Intensity (W/cm^2)
(HeNe Laser)
1
0
1
1

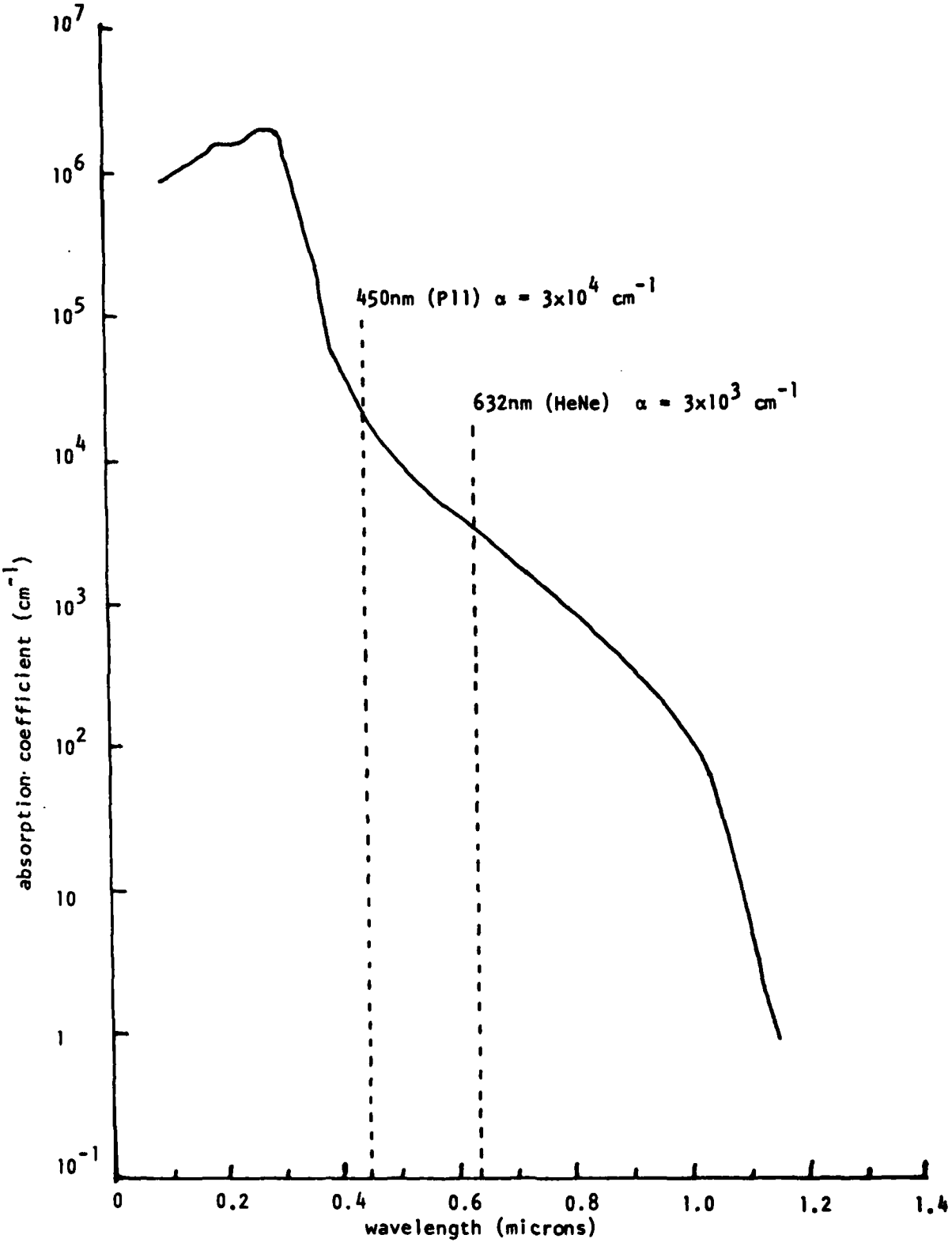


FIG. 17: Room temperature absorption coefficient vs wavelength for Silicon

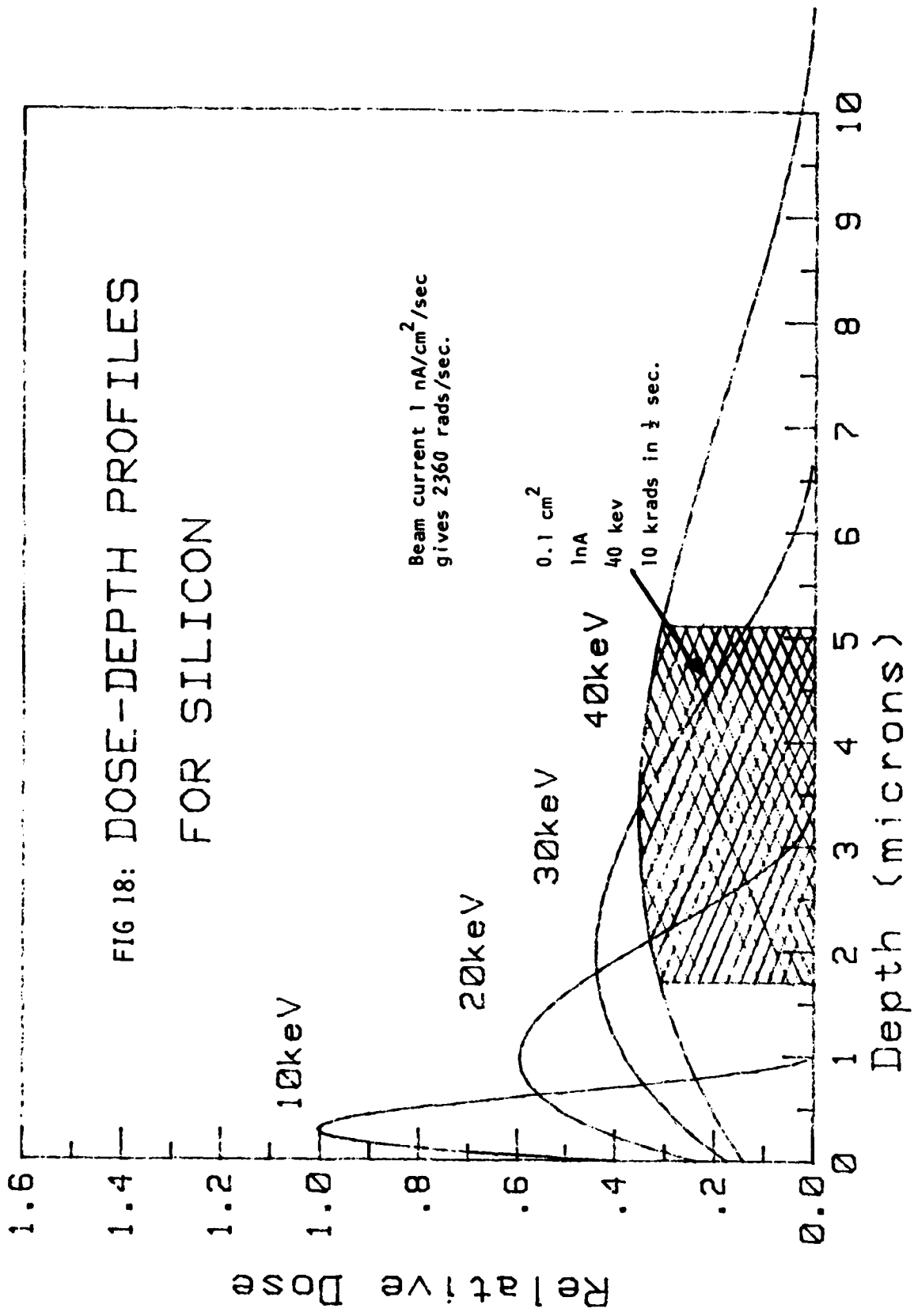


FIG 18: DOSE-DEPTH PROFILES
FOR SILICON
Beam current 1 nA/cm^2/sec
gives 2360 rads/sec.
0.1 cm^2
1nA
40 kev
10 krads in ½ sec.
10keV
20keV
30keV
40keV
Relative Dose
Depth (microns)
1.6
1.4
1.2
1.0
.8
.6
.4
.2
0.0
0 1 2 3 4 5 6 7 8 9 10

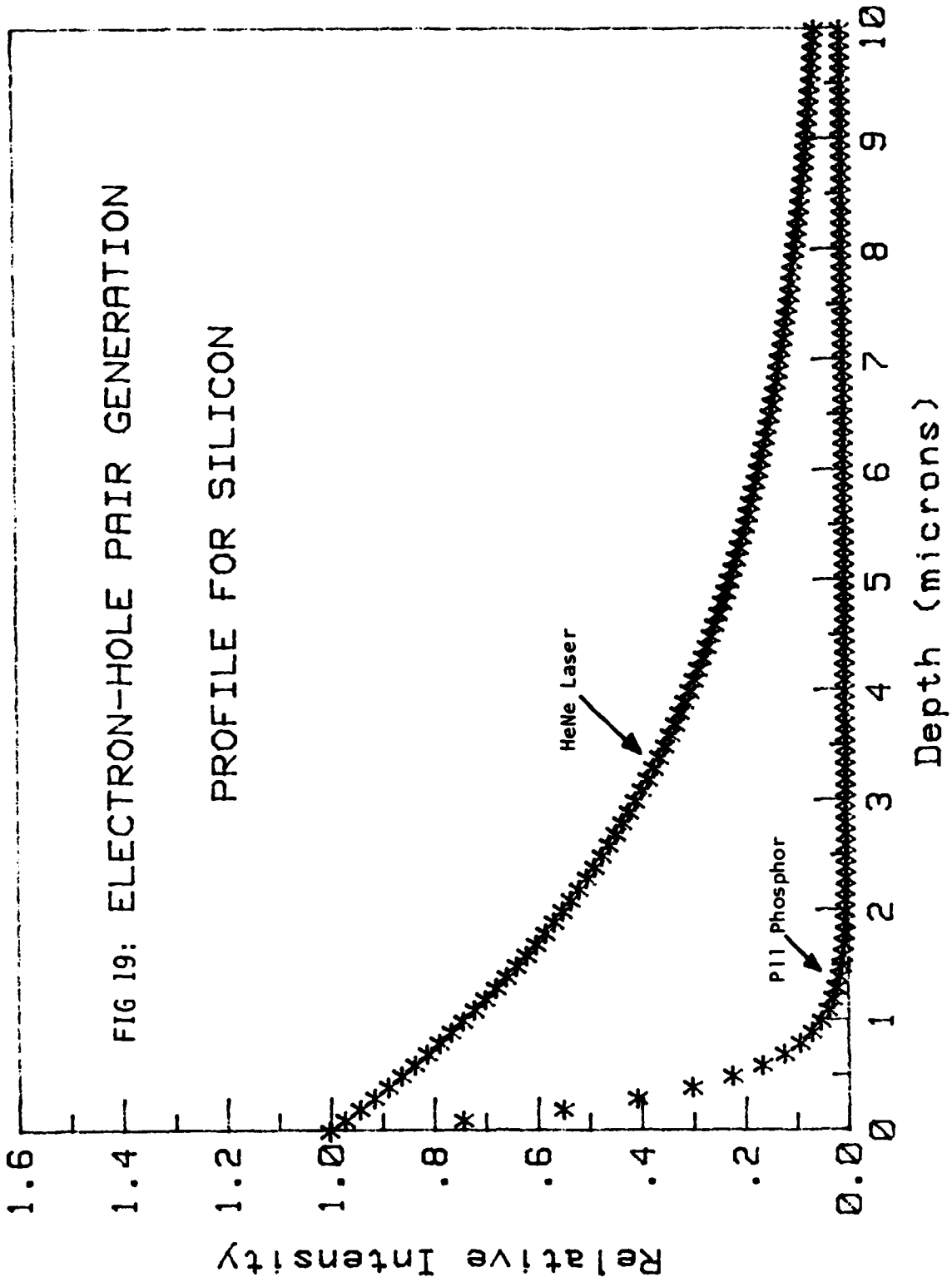


FIG 19: ELECTRON-HOLE PAIR GENERATION
PROFILE FOR SILICON
Relative Intensity
Depth (microns)
HeNe Laser
P11 Phosphor
1.6
1.4
1.2
1.0
.8
.6
.4
.2
0.0
0
1
2
3
4
5
6
7
8
9
10

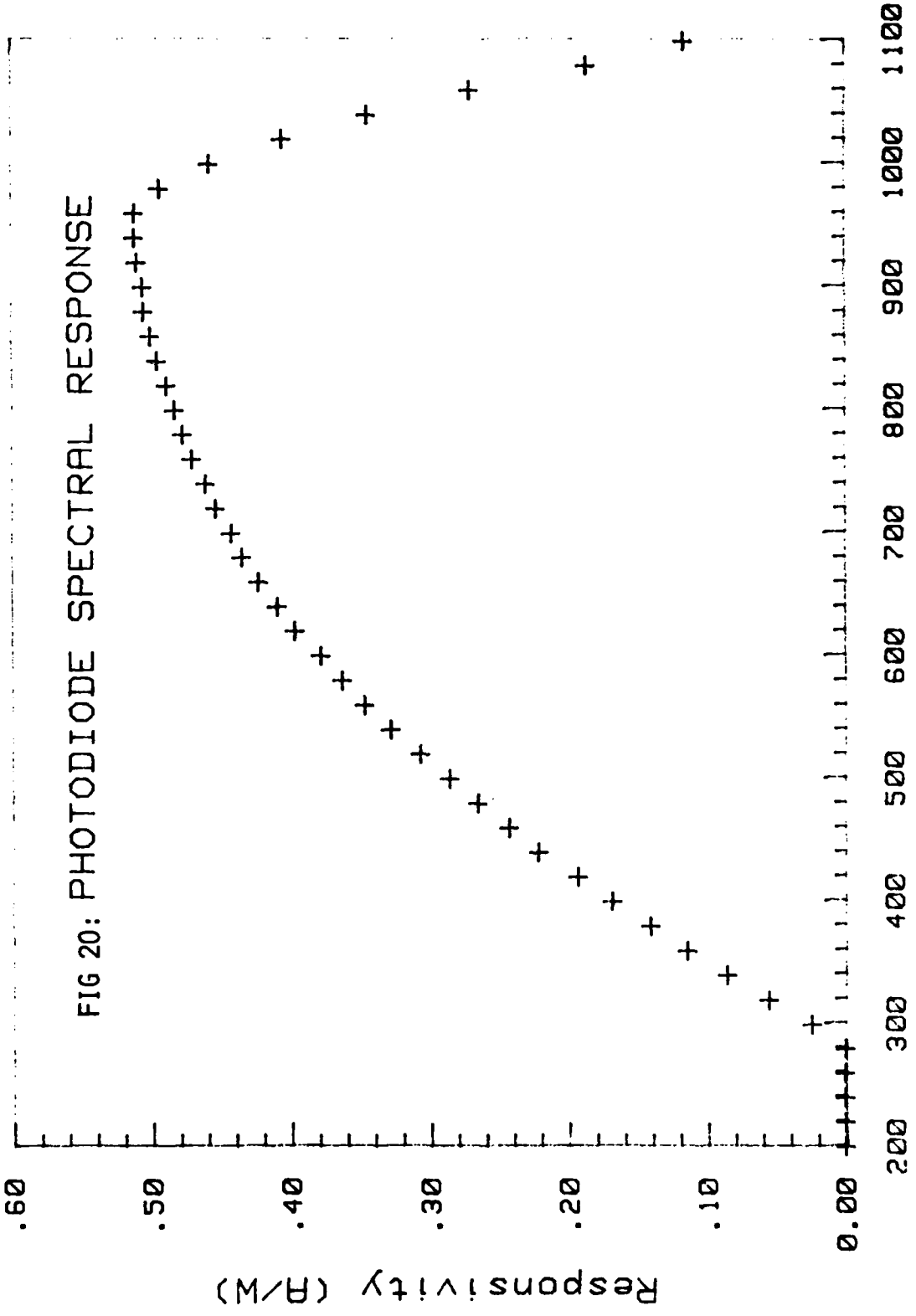


FIG 20: PHOTODIODE SPECTRAL RESPONSE
Responsivity (A/W)
.60
.50
.40
.30
.20
.10
0.00
200
300
400
500
600
700
800
900
1000
1100
Wavelength (nm)

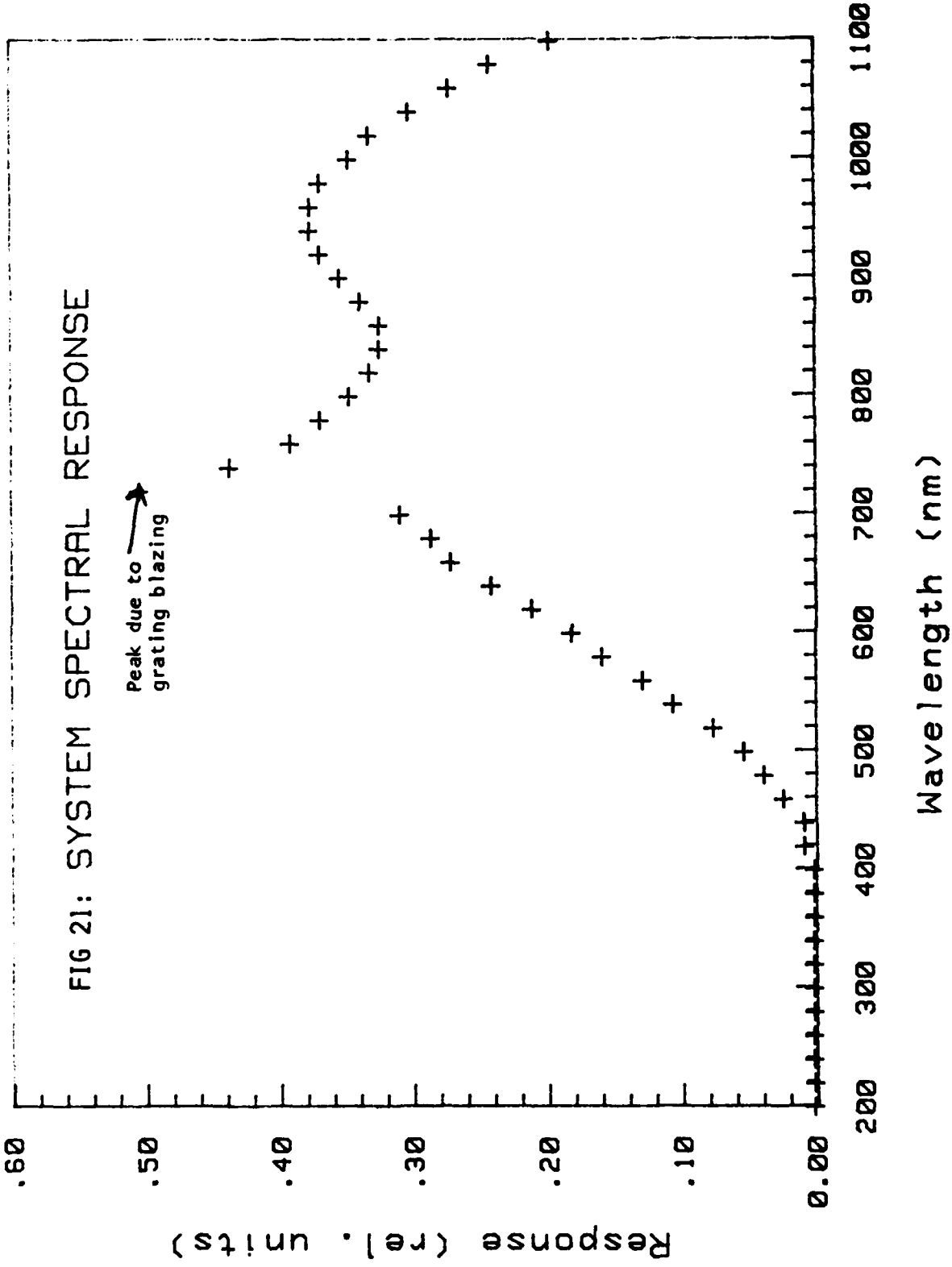


FIG 21: SYSTEM SPECTRAL RESPONSE
Peak due to grating blazing
Response (rel. units)
.60
.50
.40
.30
.20
.10
0.00
200
300
400
500
600
700
800
900
1000
1100
Wavelength (nm)

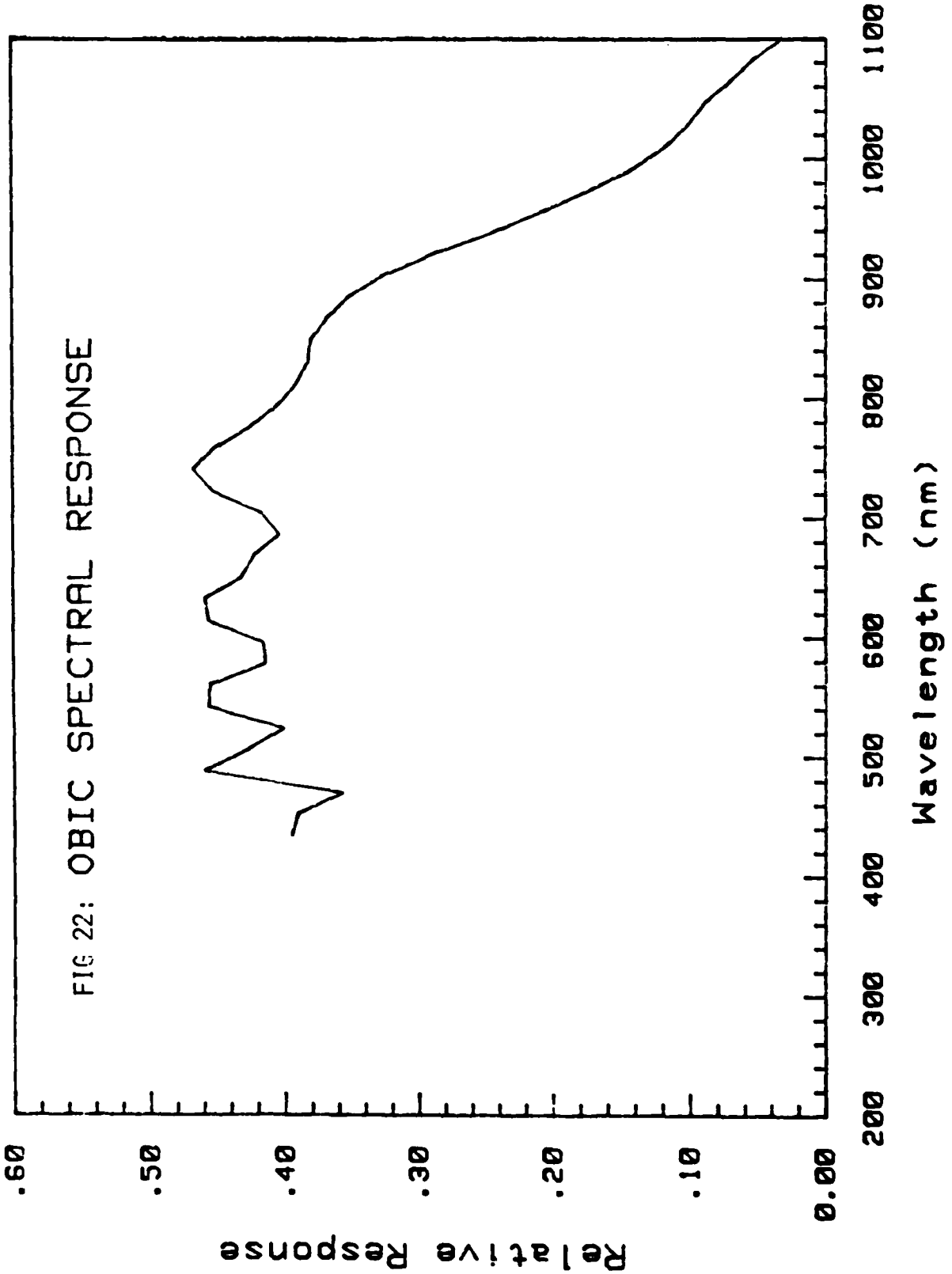


FIG 22: OBIC SPECTRAL RESPONSE
Relative Response
.60
.50
.40
.30
.20
.10
0.00
200
300
400
500
600
700
800
900
1000
1100
Wavelength (nm)

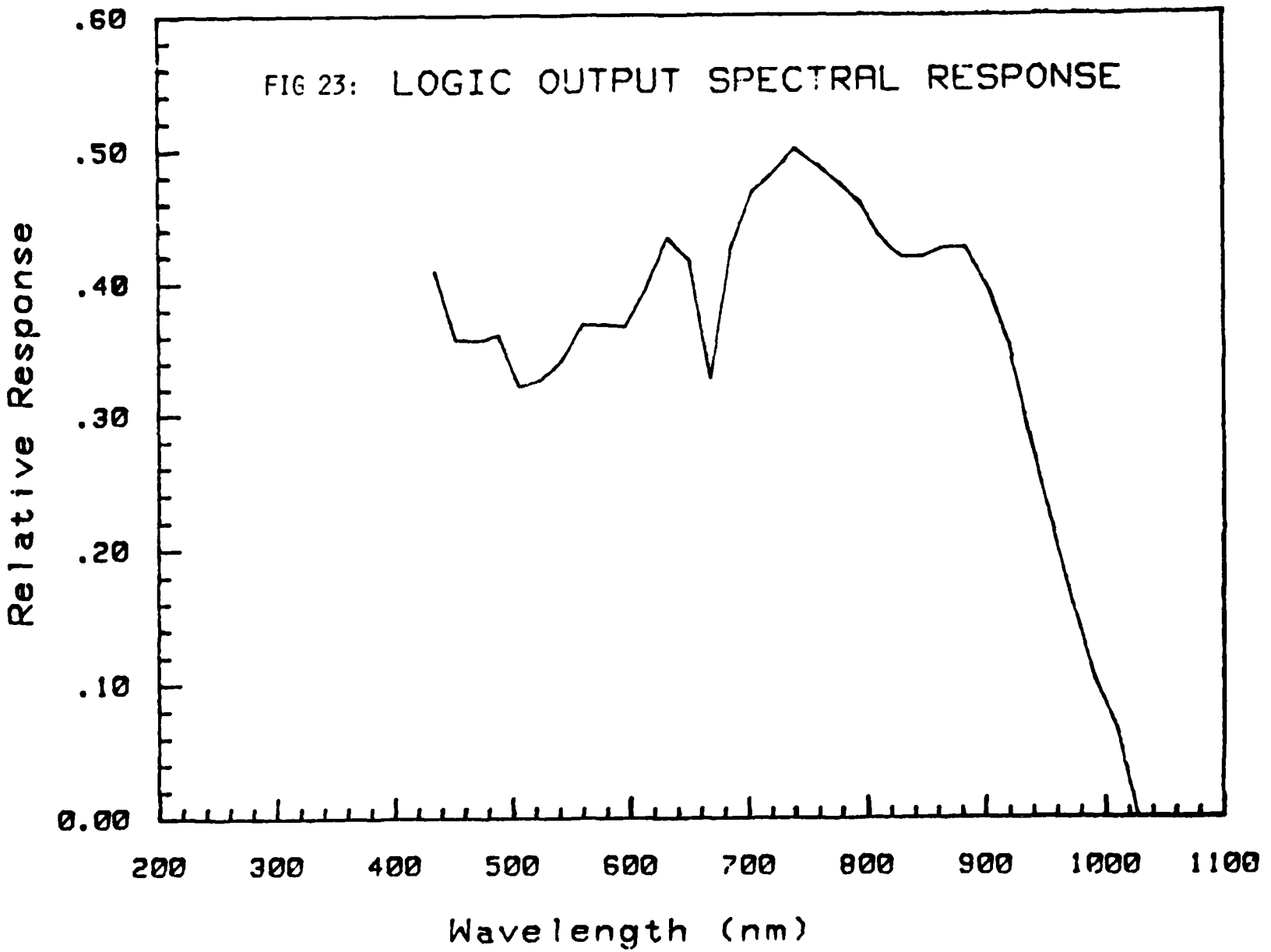
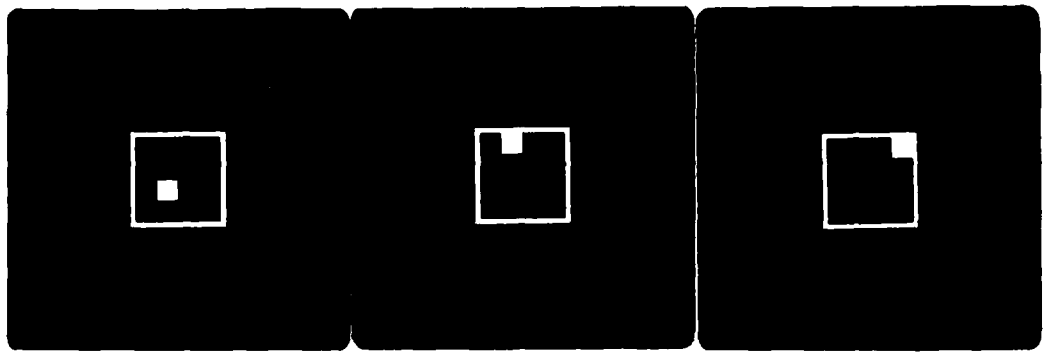


FIG 23: LOGIC OUTPUT SPECTRAL RESPONSE
Relative Response
.60
.50
.40
.30
.20
.10
0.00
200
300
400
500
600
700
800
900
1000
1100
Wavelength (nm)



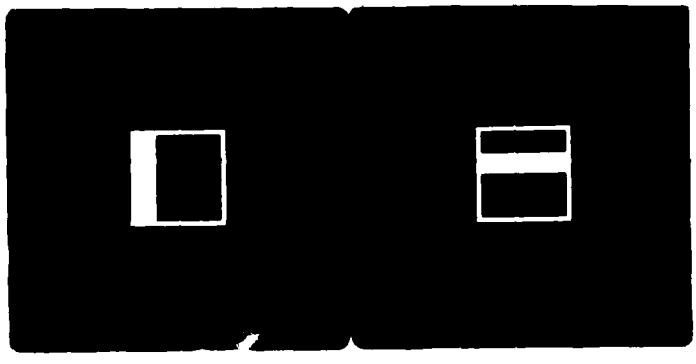


FIG. 24: a) Spot scan and XY strip search formats. Rotation and inversion of these masks gives all possible positions within 4X4 matrix

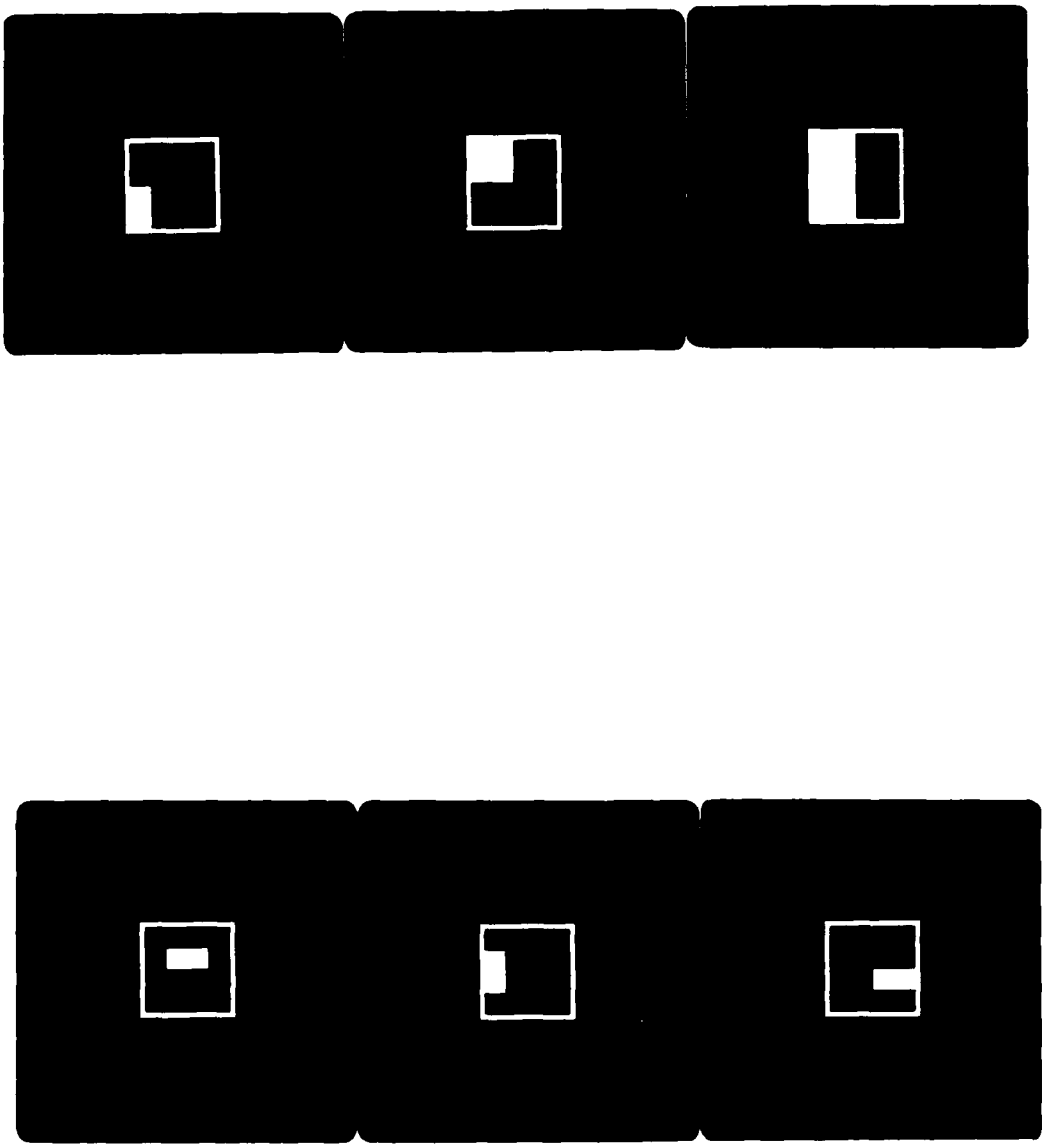


FIG. 24: b) Binary search format.
The top three masks are theoretically sufficient to locate a defective element in a 4X4 matrix with only four iterations. The bottom three masks and those of Fig. 24 a) may be used to check the fault location.

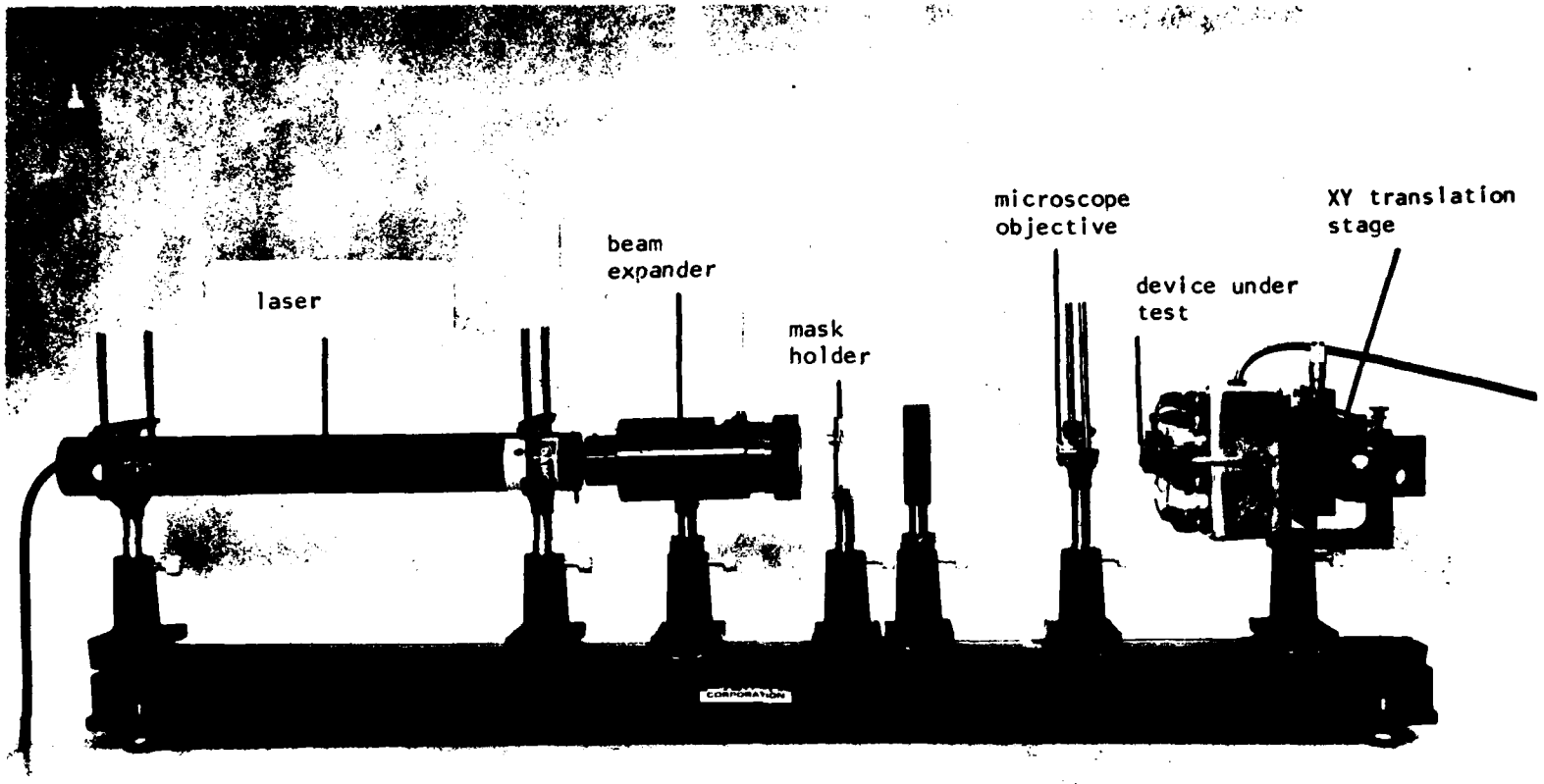


FIG. 25: OPTICAL PROJECTION SYSTEM FOR COMPARISON OF SEARCH FORMATS

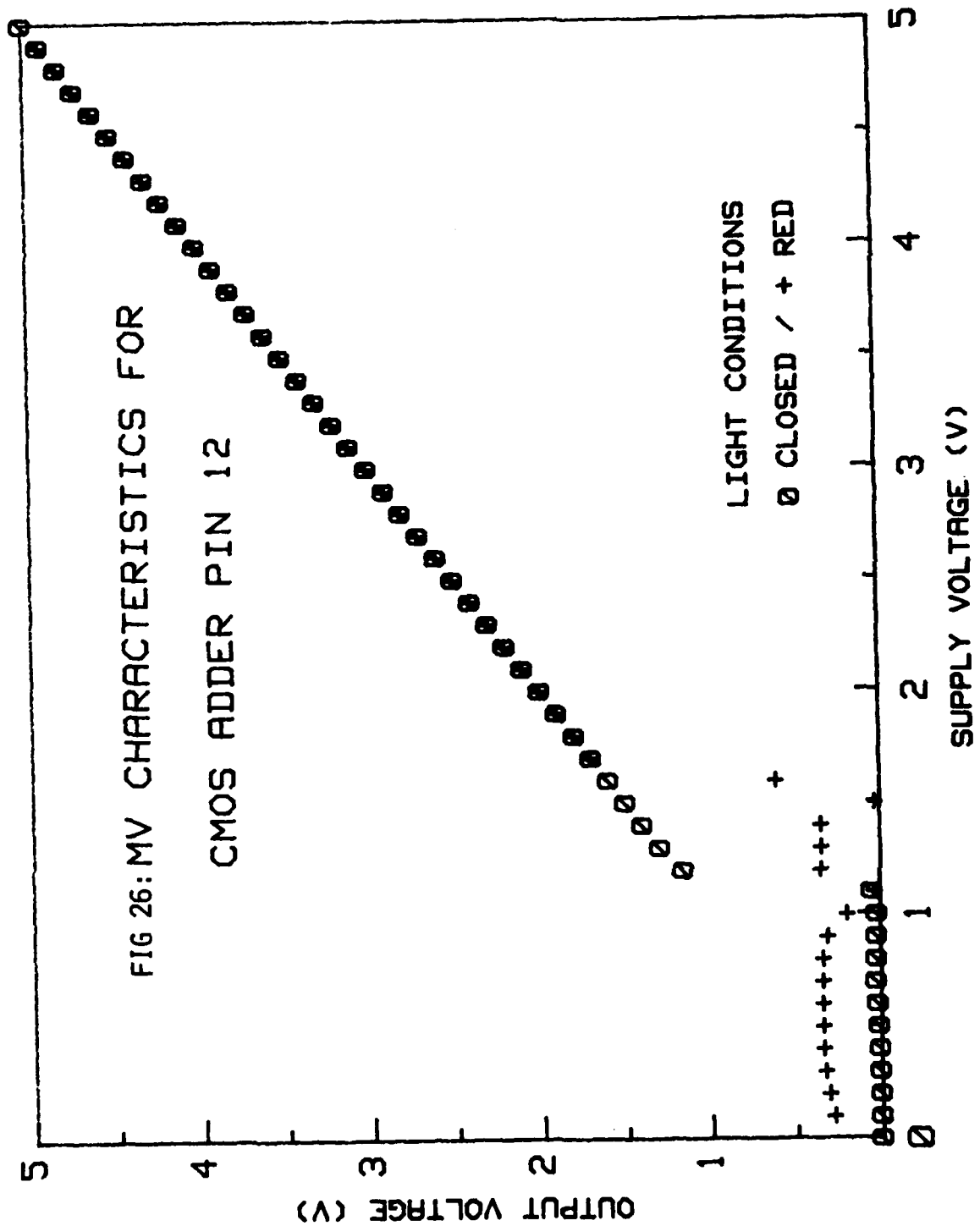


FIG 26: MV CHARACTERISTICS FOR
CMOS ADDER PIN 12
LIGHT CONDITIONS
0 CLOSED / + RED
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
0
1
2
3
4
5

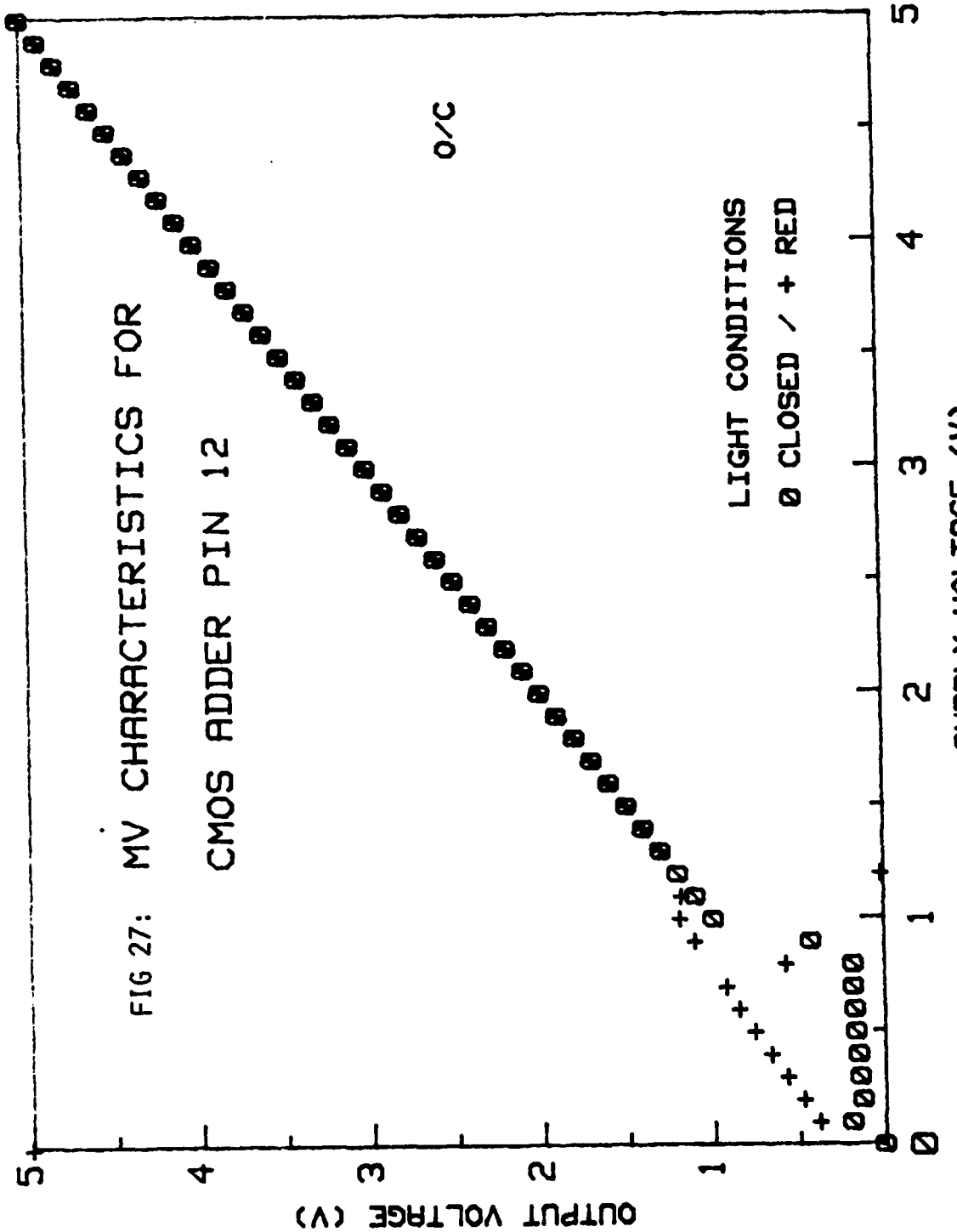


FIG 27: MV CHARACTERISTICS FOR
CMOS ADDER PIN 12
O/C
LIGHT CONDITIONS
Ø CLOSED / + RED
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
0
1
2
3
4
5

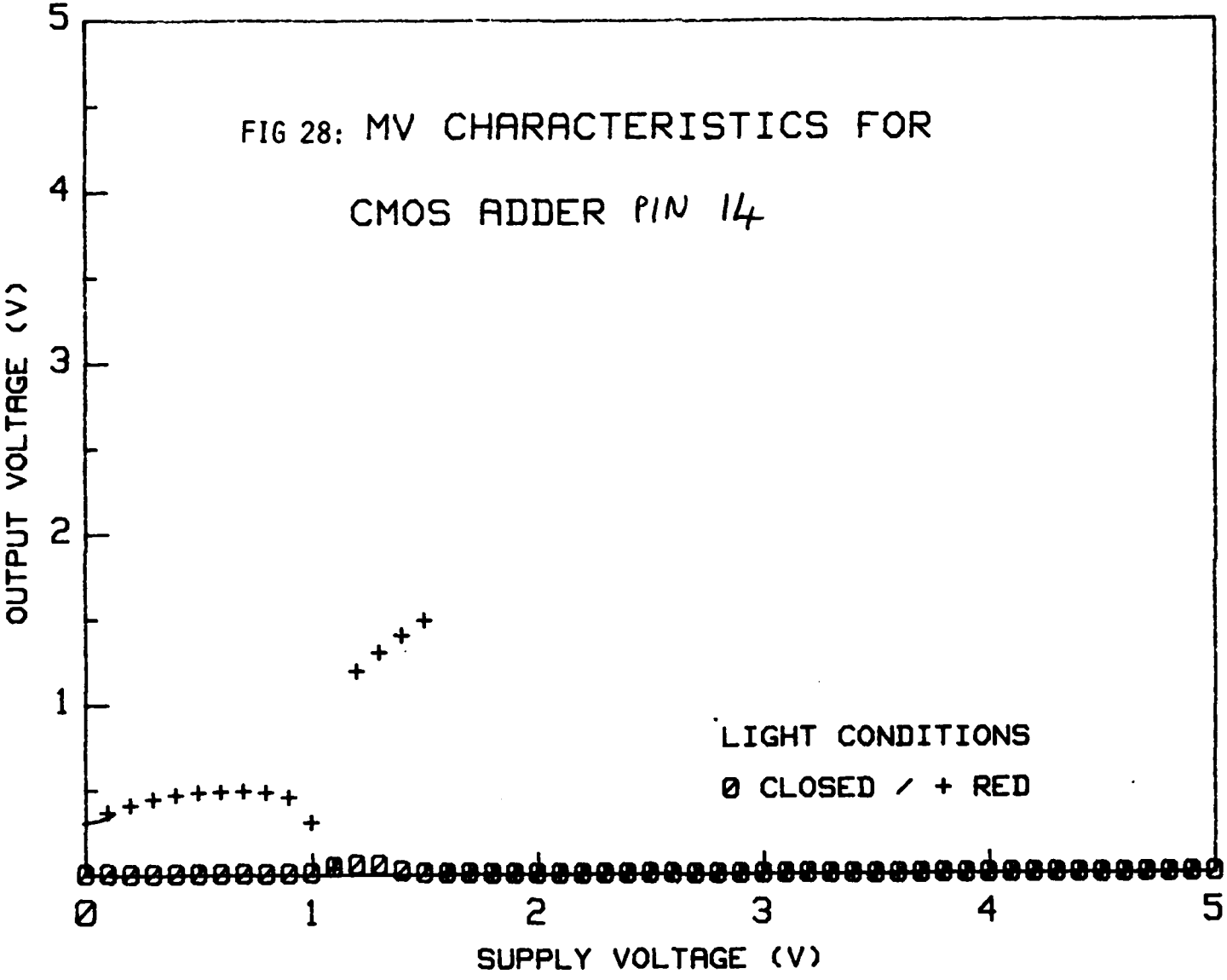


FIG 28: MV CHARACTERISTICS FOR
CMOS ADDER PIN 14
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
LIGHT CONDITIONS
0 CLOSED / + RED
0
1
2
3
4
5

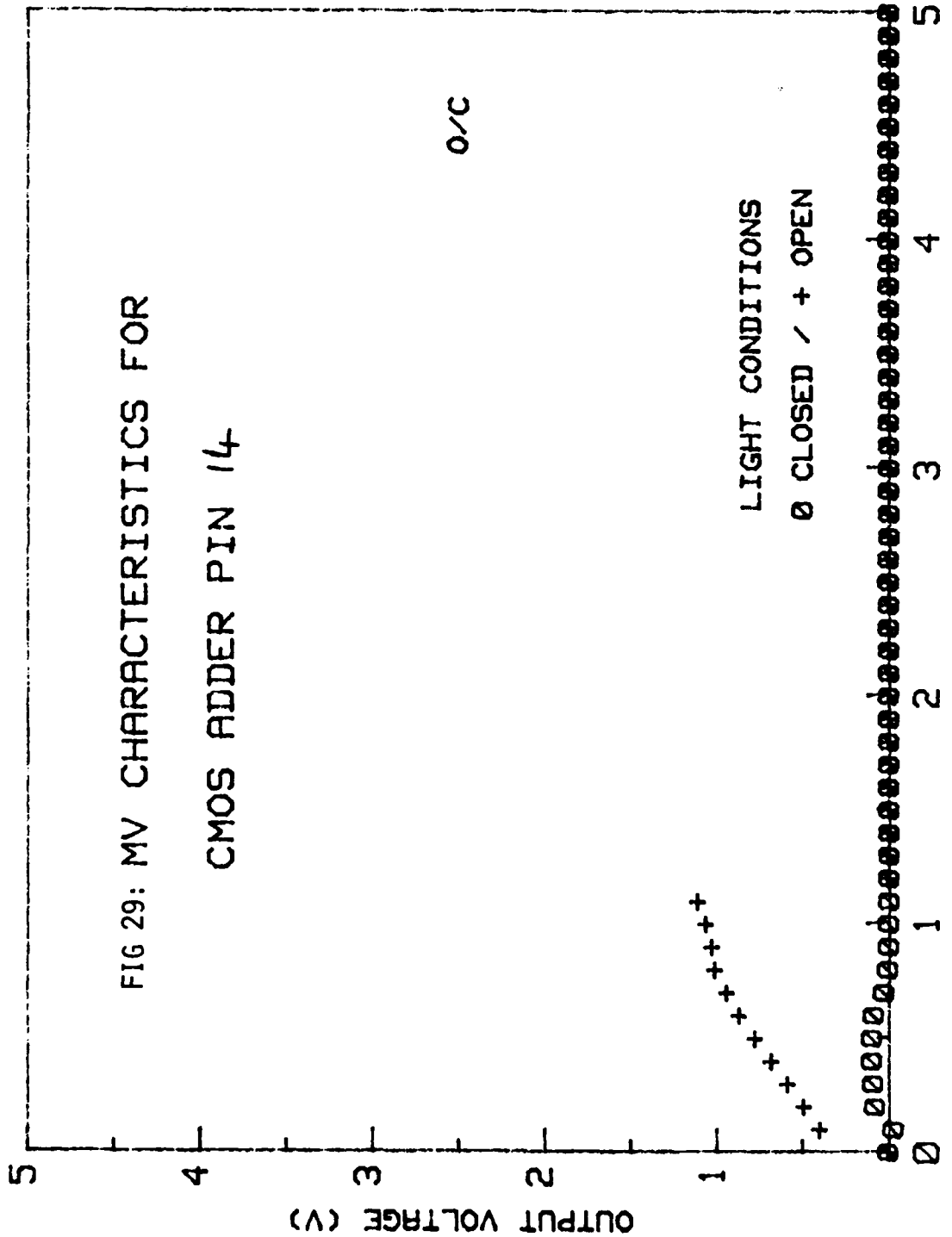
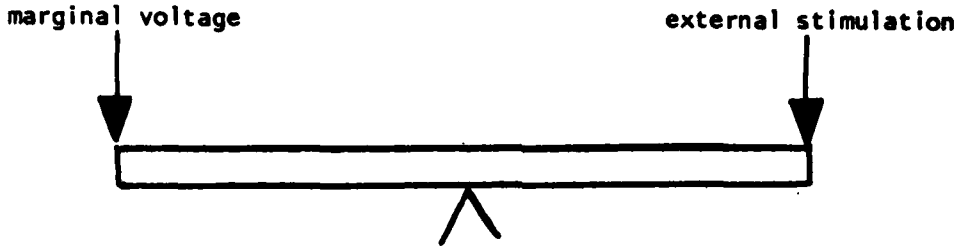


FIG 29: MV CHARACTERISTICS FOR
CMOS ADDER PIN 14
O/C
LIGHT CONDITIONS
Ø CLOSED / + OPEN
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (V)
0
1
2
3
4
5



increasing intensity

SUPPLY VOLTAGE		
1.0V	1.1V	1.2V
00000	11010	11010
00000	11010	11010
00000	00000	00110
00000	00000	00000
00000	00000	00000
11100	00000	00000
11110	00000	00000
11110	10000	00000

(correct output word is 11010)

FIG 30: Illustration of relationship between marginal voltage and level of external stimulation.

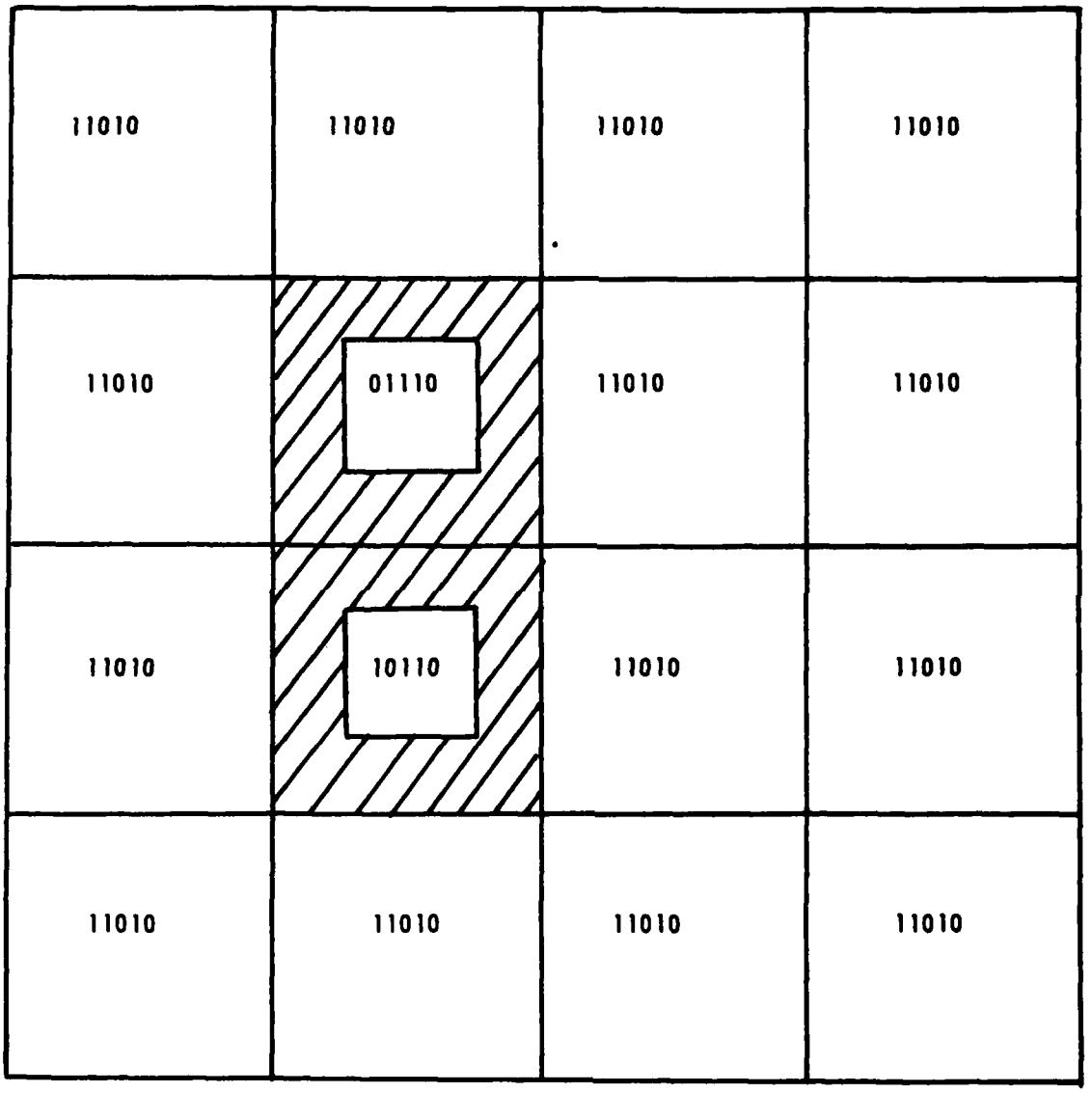


FIG. 31: Location of circuit weak spots using the 'spot scan' or raster search format.

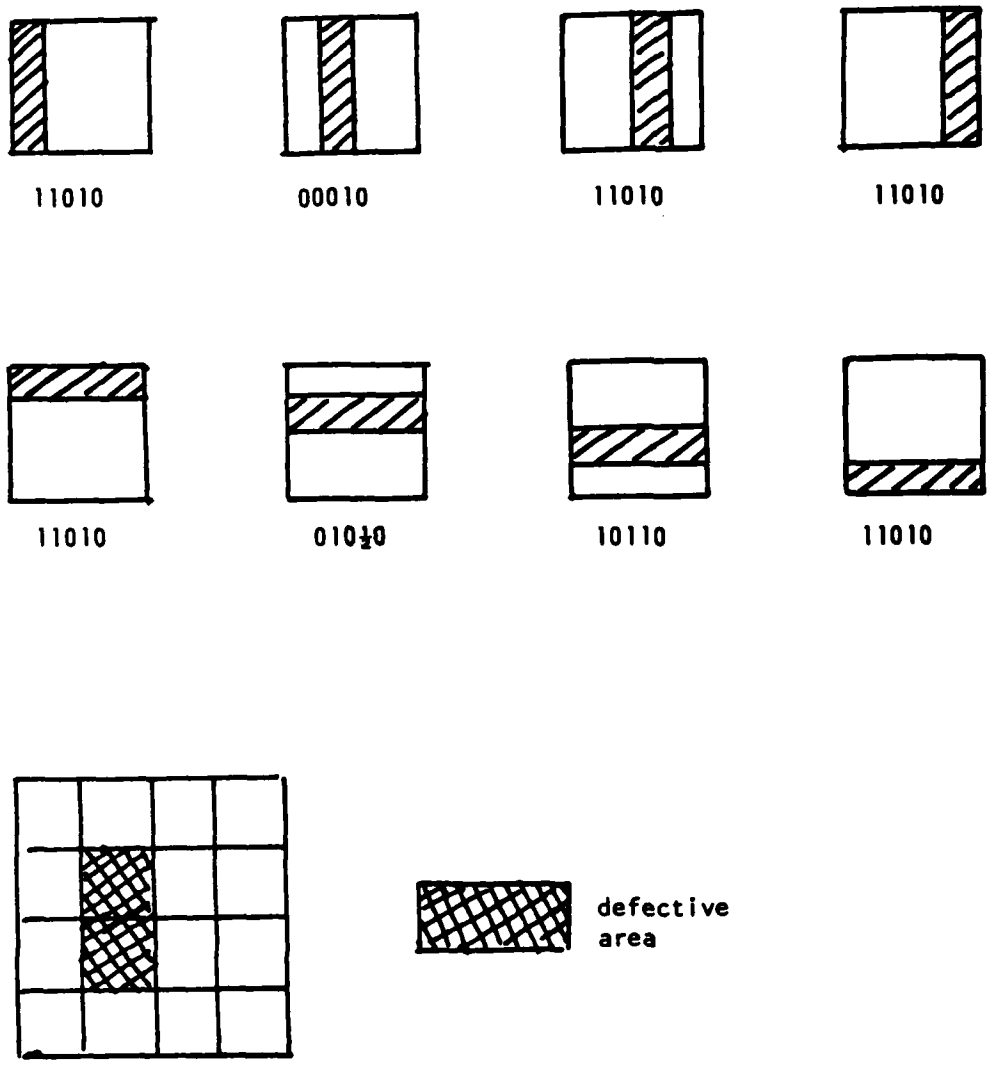


FIG. 32: Location of circuit week spots using XY strip search format.

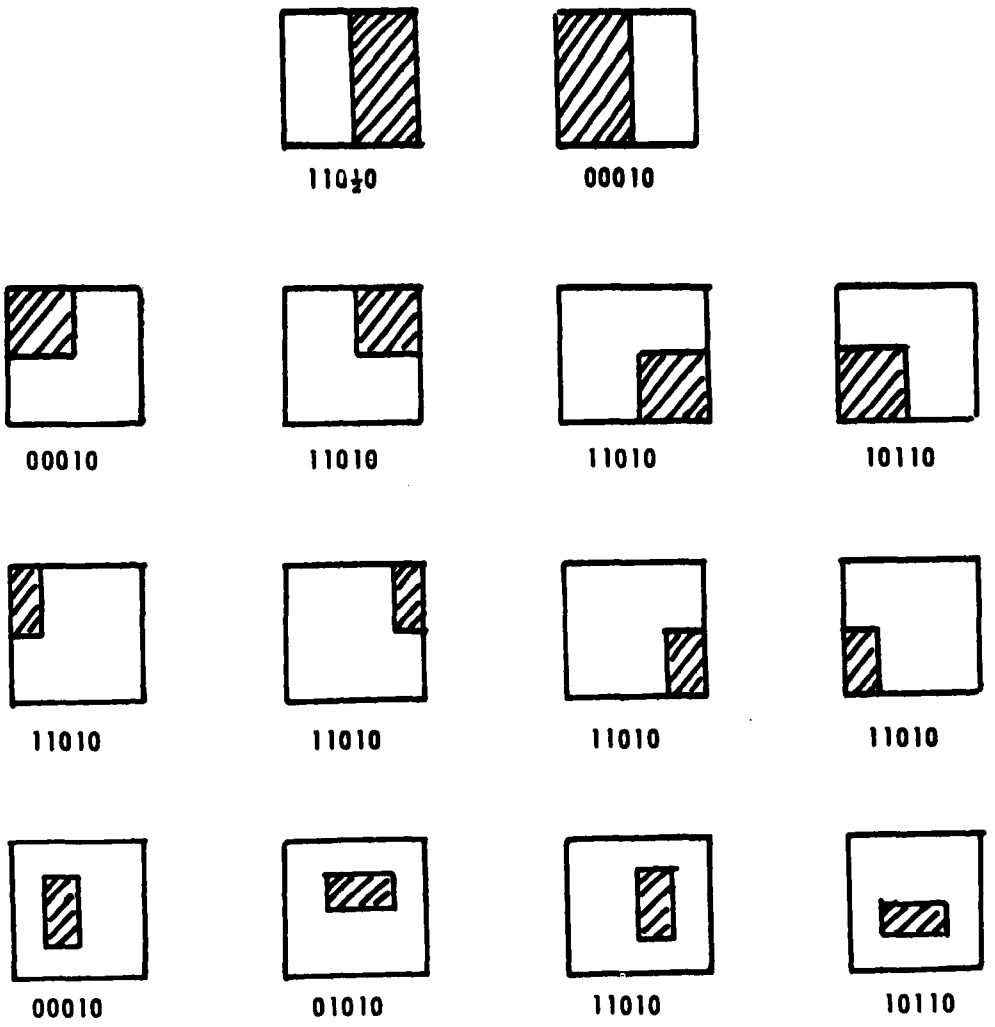


FIG 33: Location of circuit weak spots using binary search format.

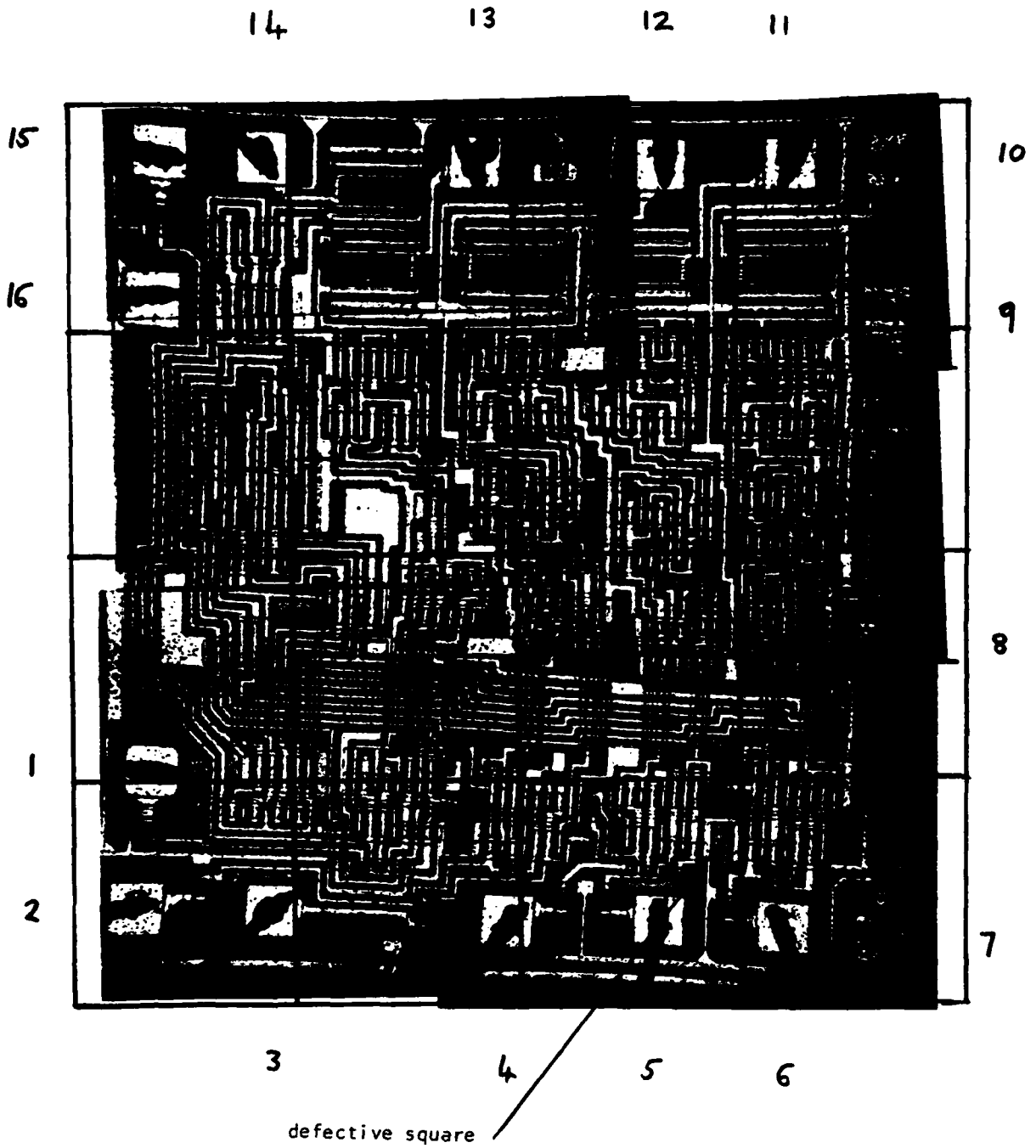


FIG. 34: Optical micrograph of CMOS adder

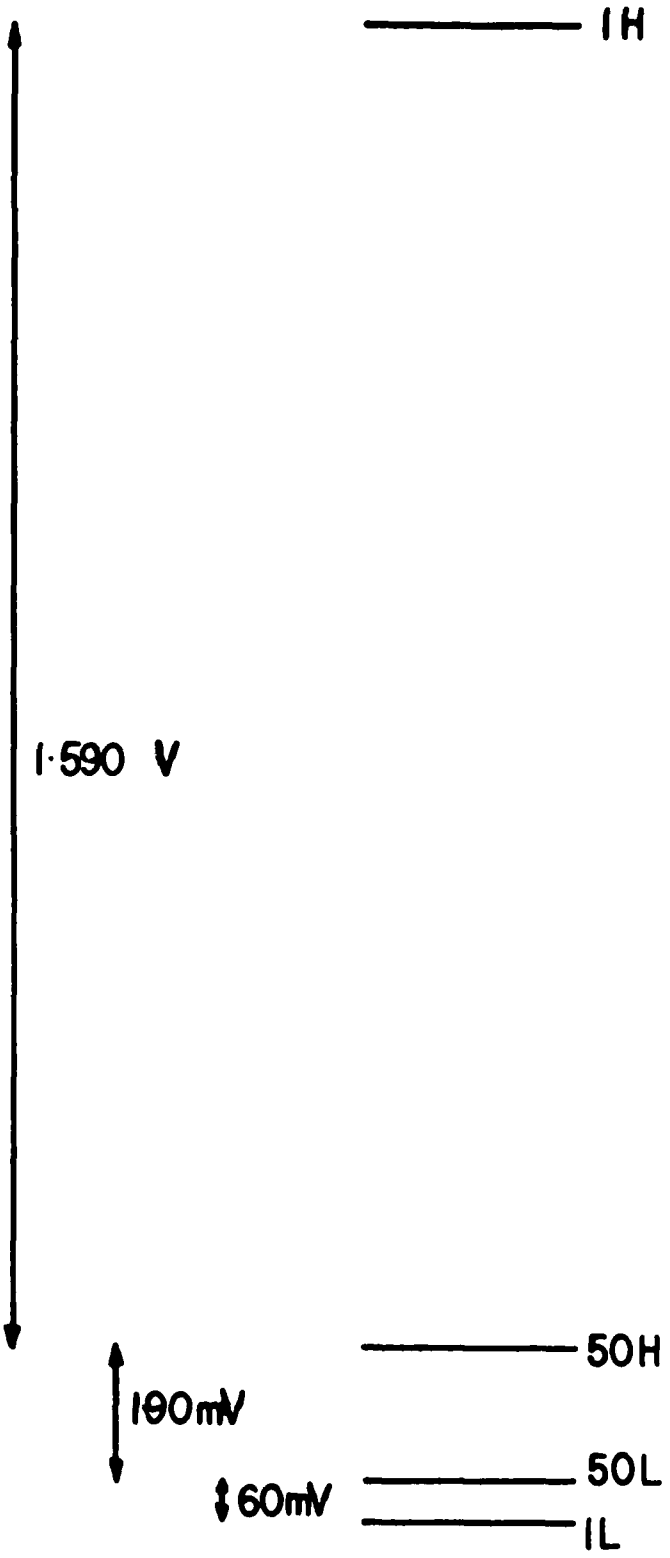
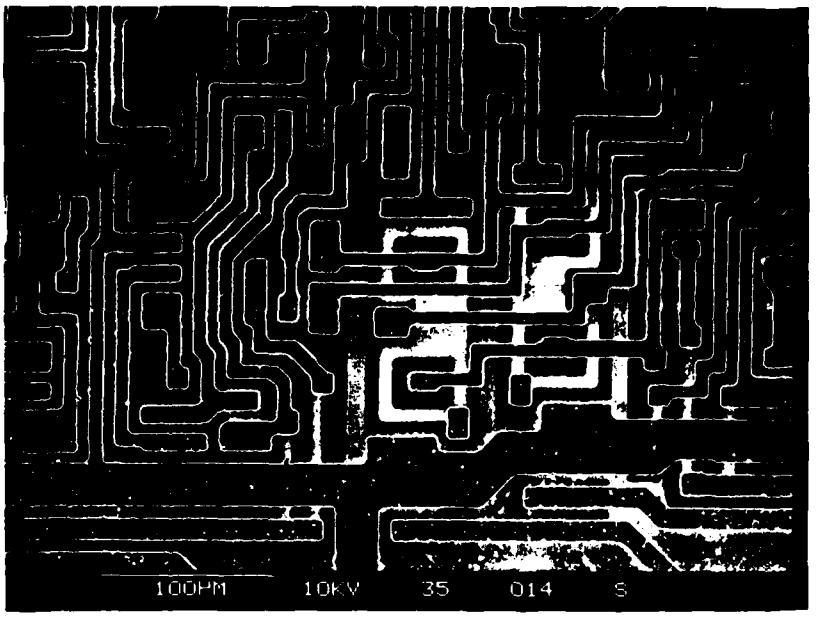
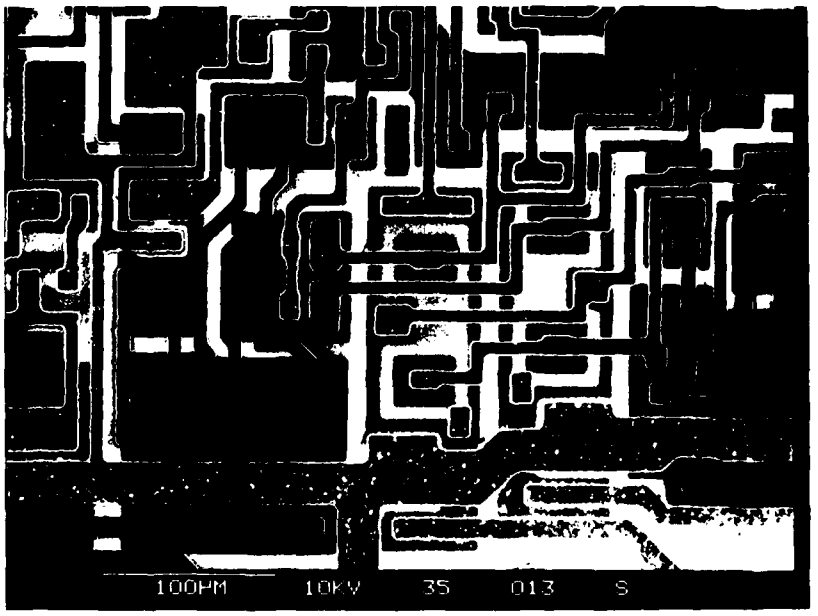


Fig. 35: Marginal voltage distribution for TTL Comparator

FIG.36: DEFECT LOCATION IN TTL COMPARATOR

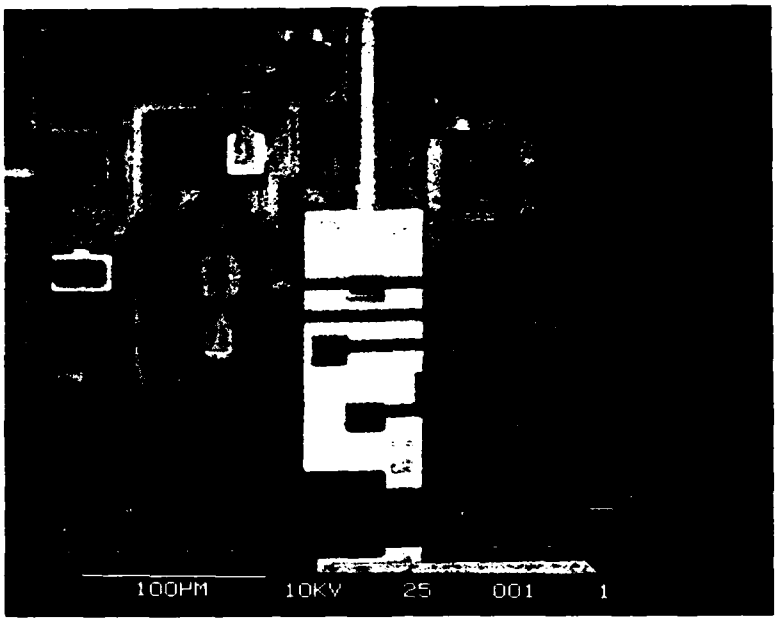


a) Secondary image of area of TTL 4-bit comparator.

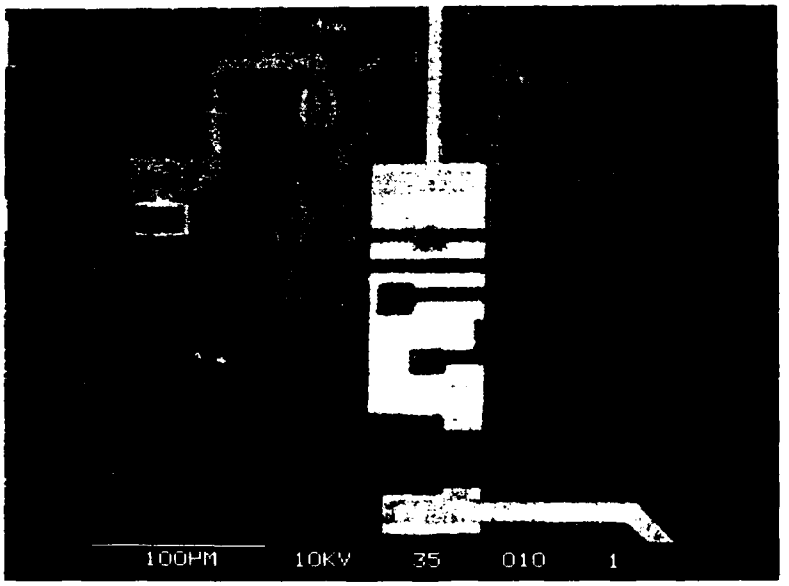


b) as (a) with voltage contrast: Black +'ve White -'ve

FIG 37: VOLTAGE CONTRAST IN THE SEM

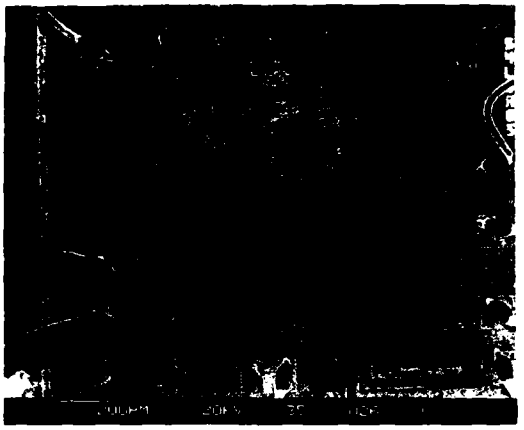


a) Defective area of circuit with anomalous marginal voltage.



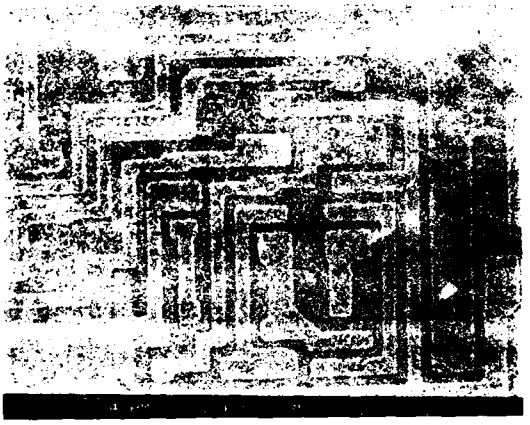
b) Similar area of normal circuit.

FIG 38: VOLTAGE CONTRAST IN THE SEM



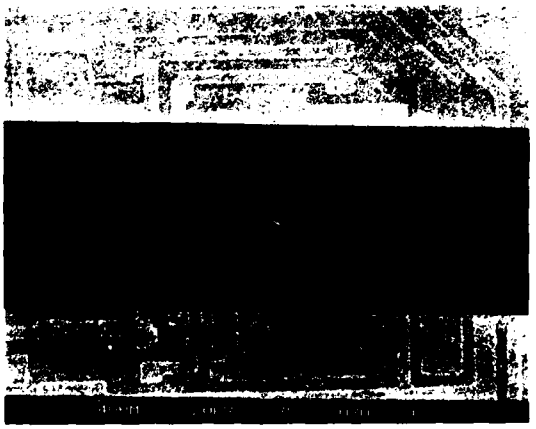
a) 4.25V

b) 4.15V



c) 4.25V

d) 4.15V

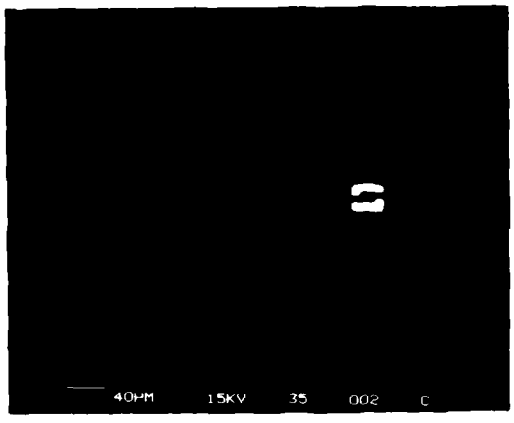


e) 4.05V

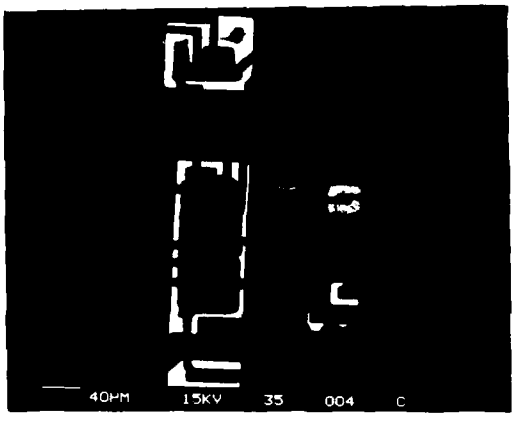
f) 4.20V

FIG. 39: SEM location of defective area in faulty circuit under marginal voltage conditions.

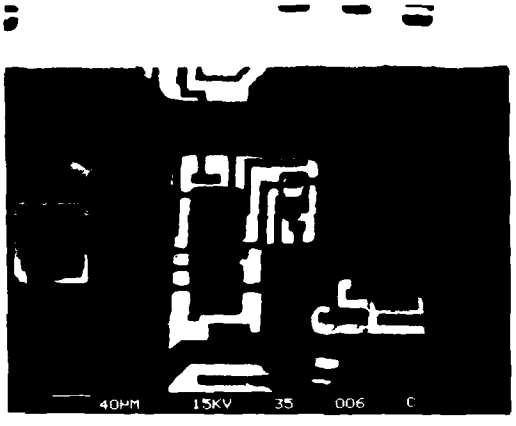
a) 2.90V



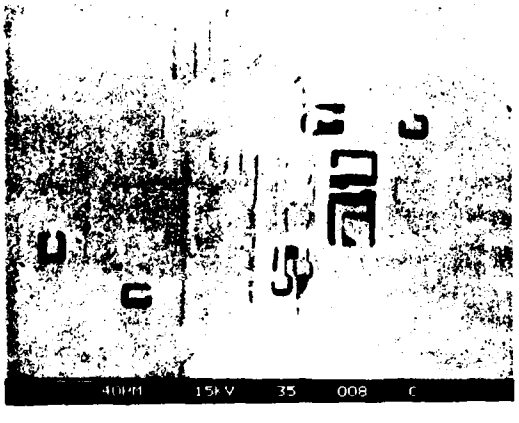
b) 292V



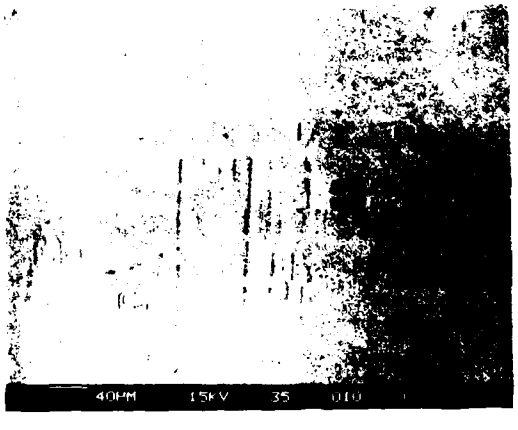
c)2.94V



d) 2.96V



e) 2.98V



f) 3.00V

FIG. 40: SEM location of circuit weak spots in a normal circuit under marginal voltage conditions.

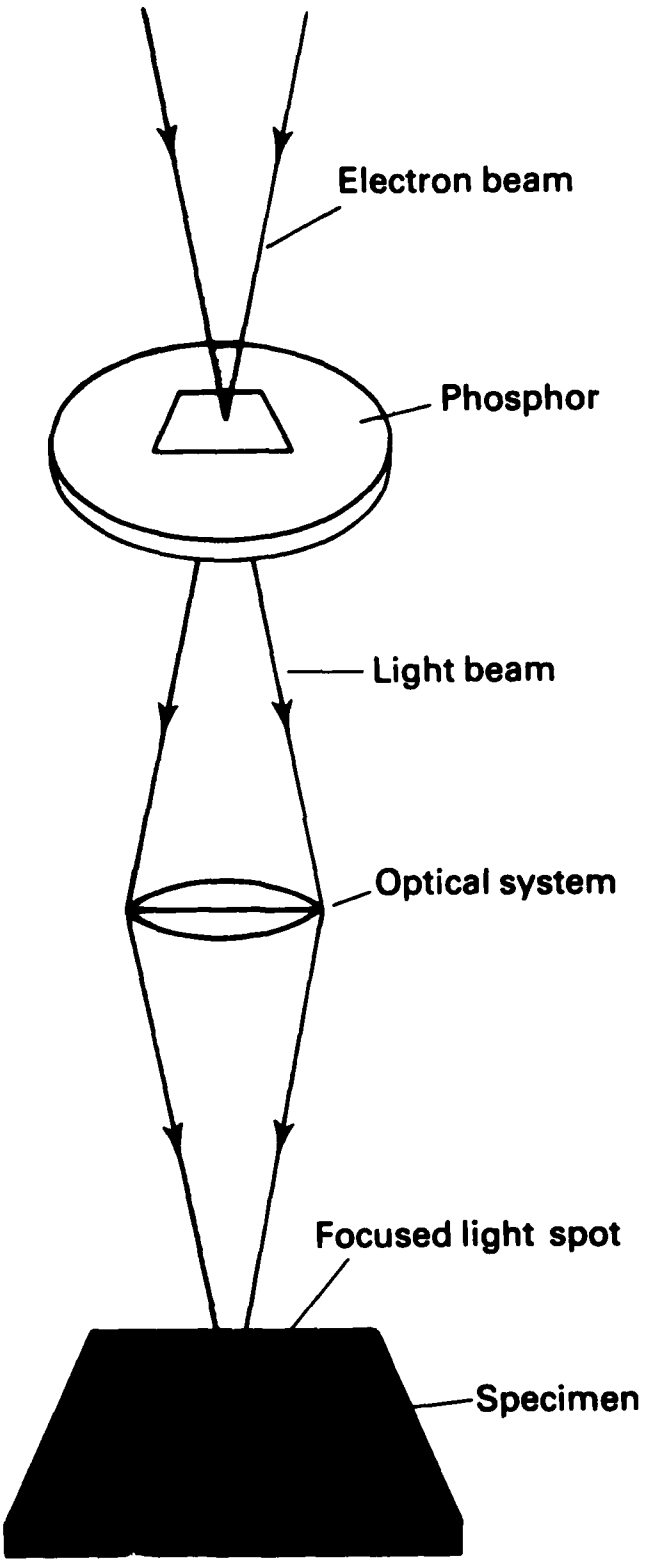


FIG 41: SOMSEM SYSTEM DIAGRAM

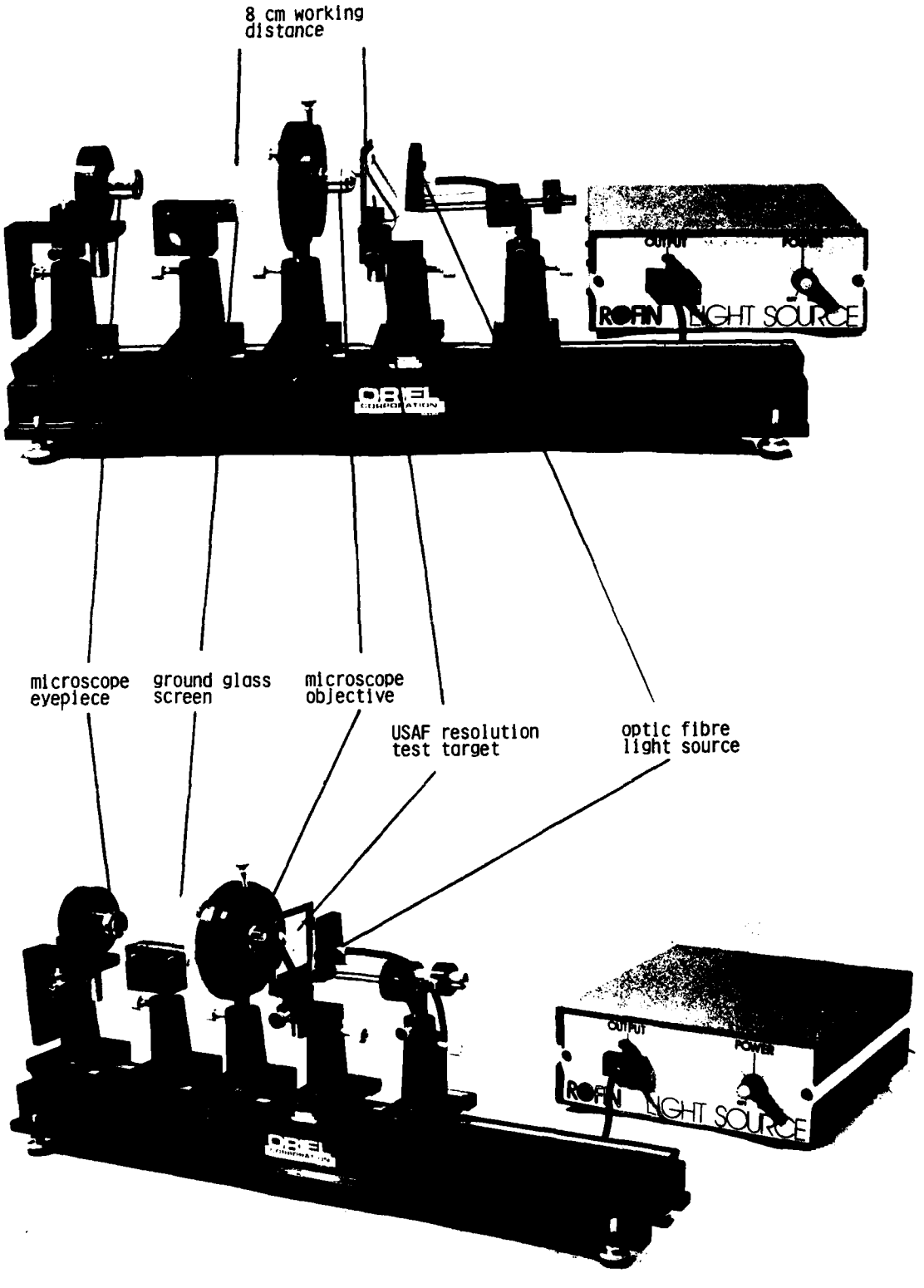


FIG.42: SOMSEM simulation system

Table 1

Results of microscopic objectives using SOMSEM simulation projection system (working distance scan)

Microscope Objective	X10	X20	X40
Field of view	6 x 6 mm	2 x 2 mm	750 x 750 μ
* demagnification	2.7	7.5	14
Resolution	<4 μ	<2.5 μ	<1.5 μ
Useful magnification range (includes SEM magnification)	25-250X	100-400X	200-600X

*equivalent to:
scanned area of phosphor screen/scanned area on specimen

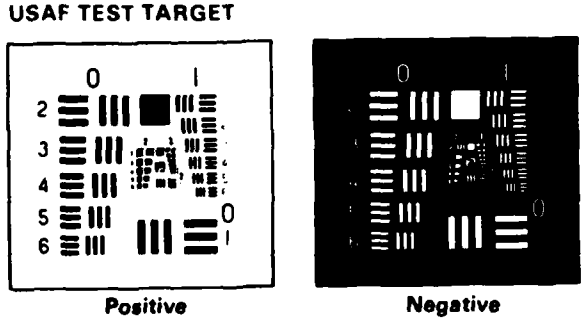
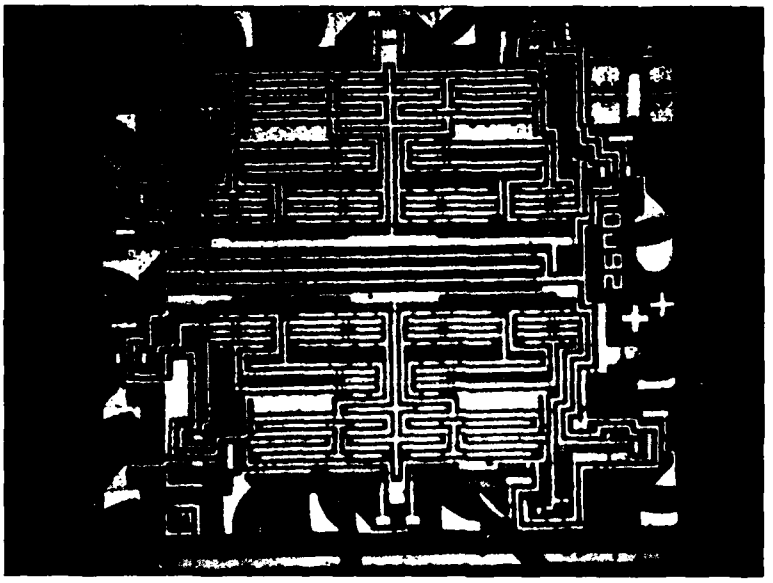


FIG. 43: USAF Test Target



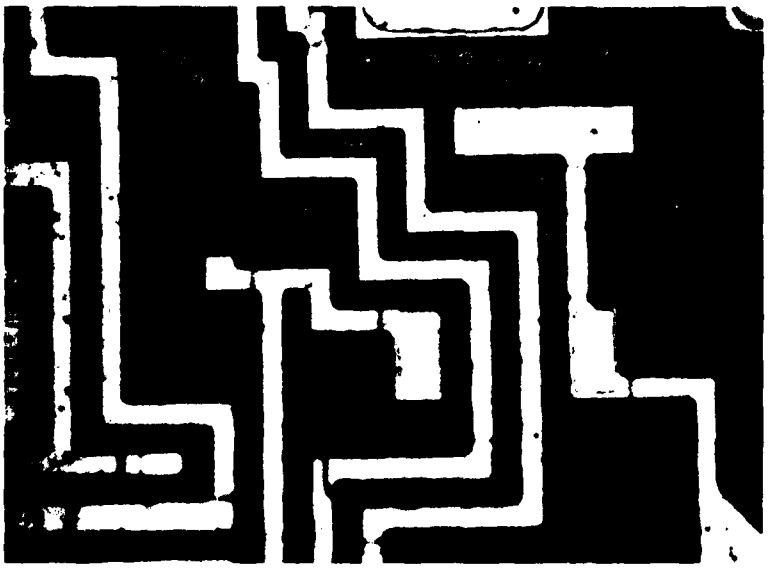


FIG. 44: Conventional optical reflection micrographs of a CMOS silicon device. The bright areas correspond to the aluminium metallization pattern, magnifications as for *Fig.* 45.

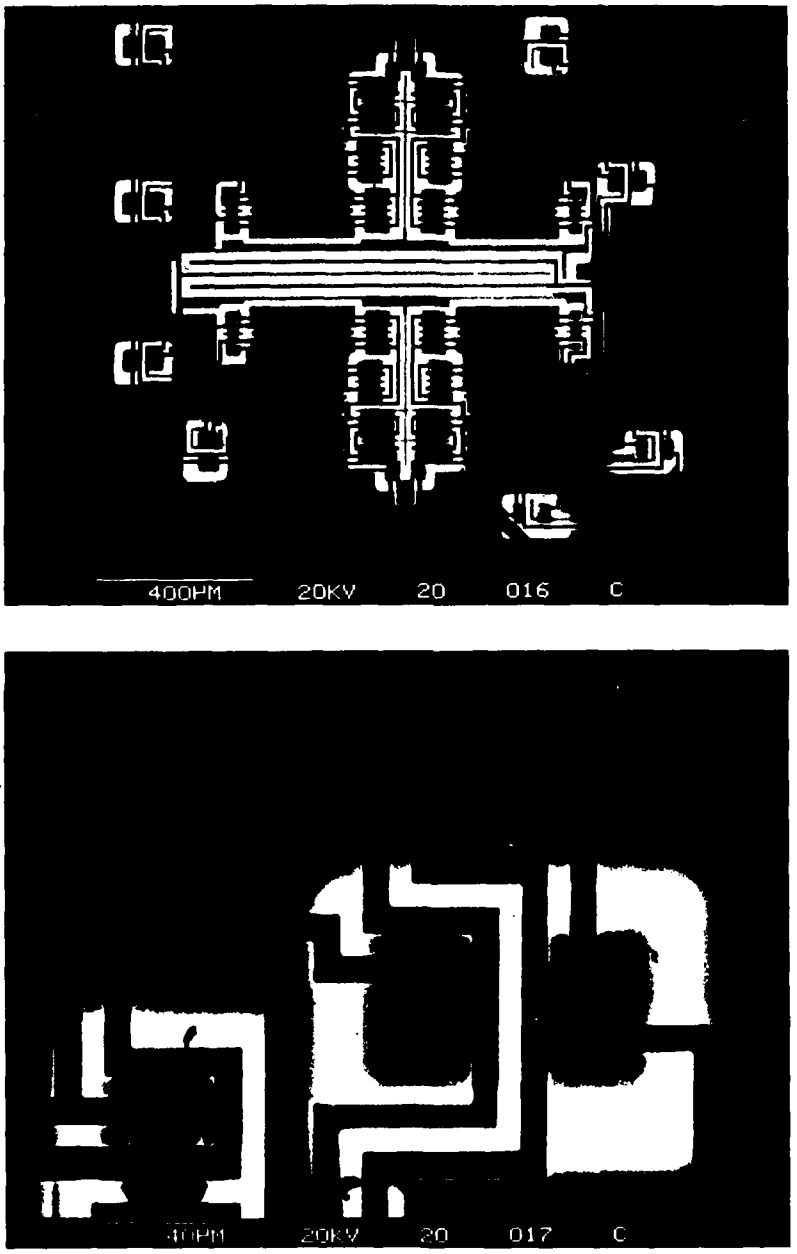
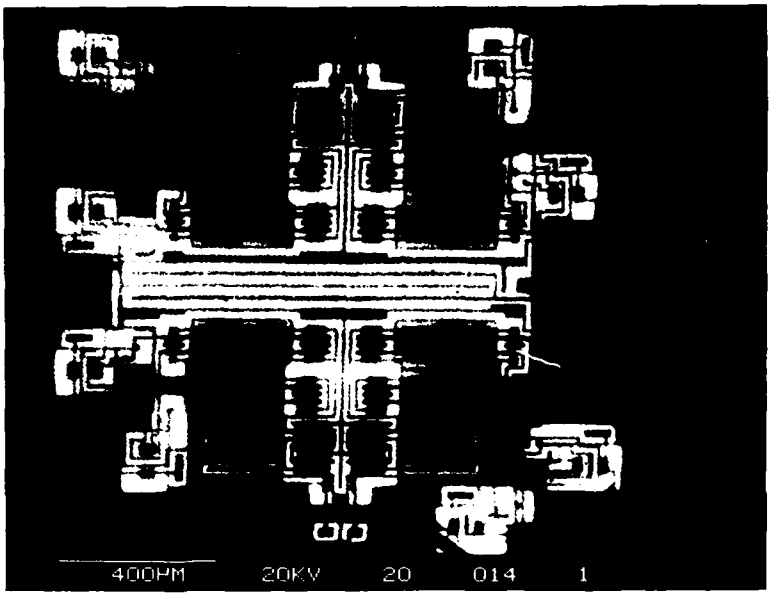


FIG. 45: SEM EBIC images of the same device. The bright areas correspond to sub-surface junctions whereas the metallization pattern is black.

N.B. The device is completely inoperative after imaging.



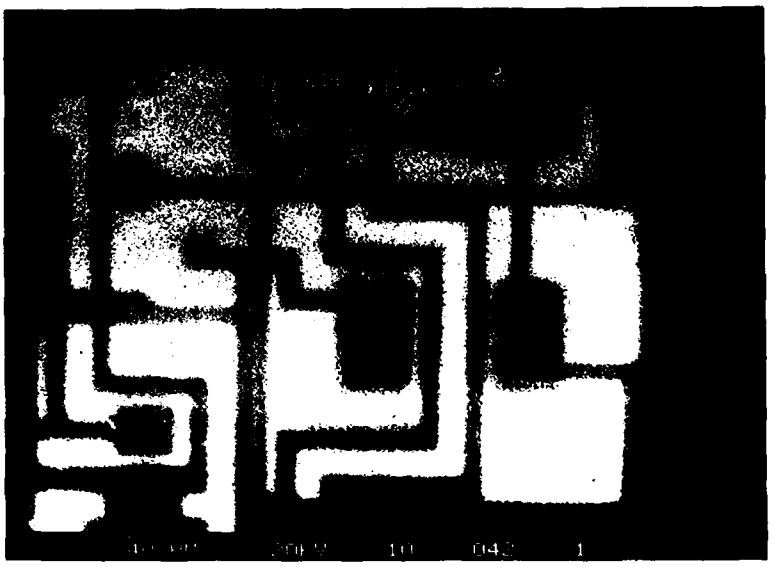


FIG. 46: SOMSEM OBIC images of the CMOS device. Additional junctions show as a result of the greater penetration depth of the optical beam (it is not absorbed by the passivating layer). The 'speckly contrast' is due to the phosphor grain size. Magnifications as for Fig. 45.

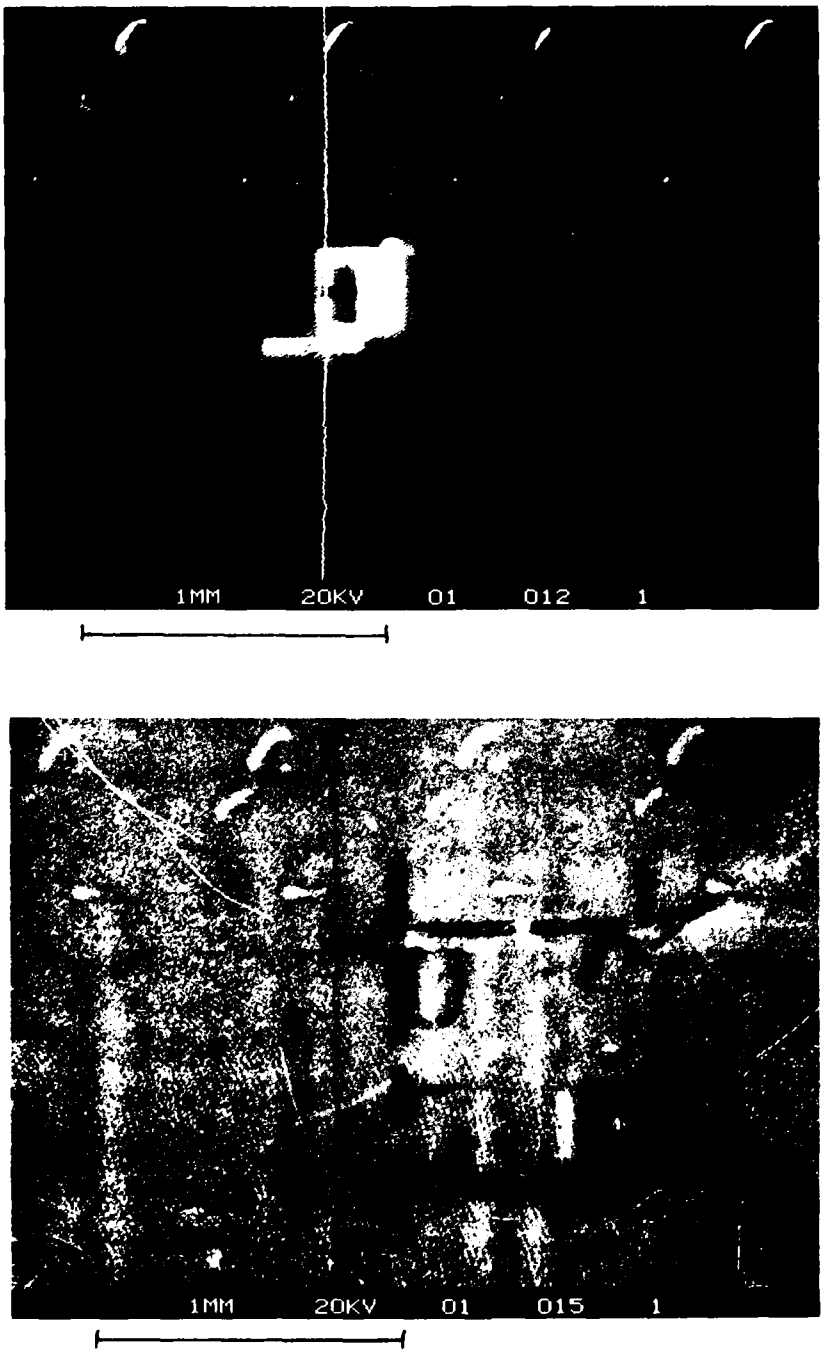


FIG. 47: POSITIVE AND NEGATIVE VERSIONS OF LOGIC STATE MAP SUPERIMPOSED ON OBIC IMAGE

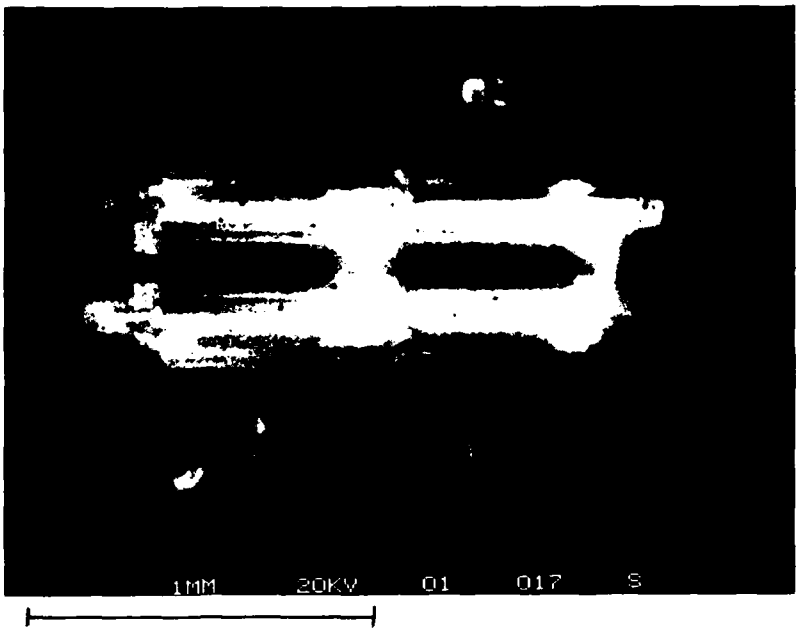


FIG. 48: OBIC IMAGE OF MOS DEVICE WITH FOUR GATES

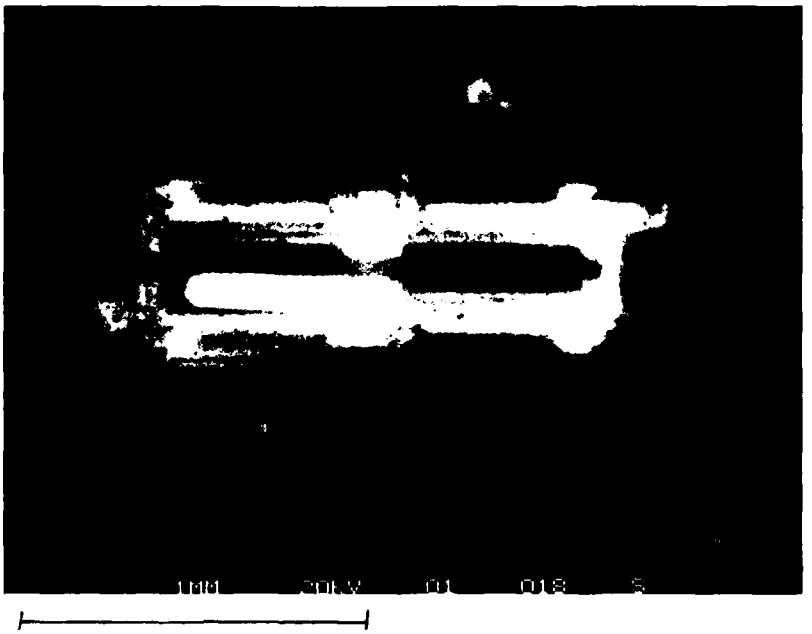


FIG. 49: OBIC IMAGE WITH THE OUTPUT OF ONE OF THE GATES SUPERIMPOSED

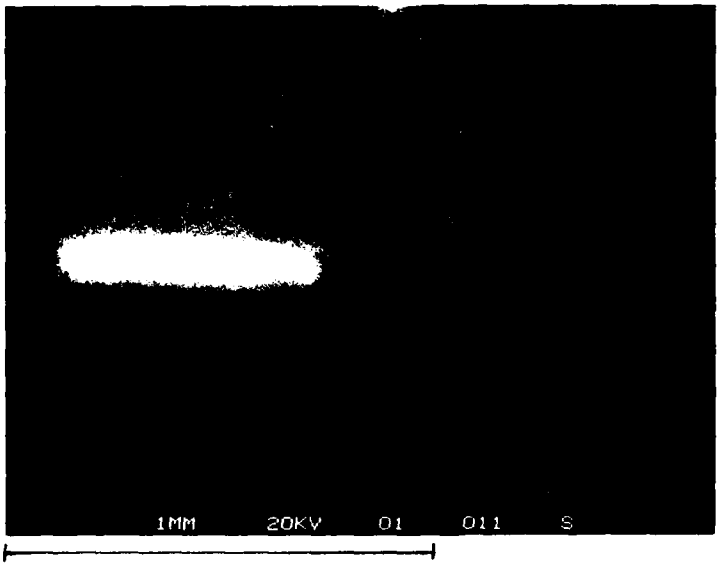


FIG. 50

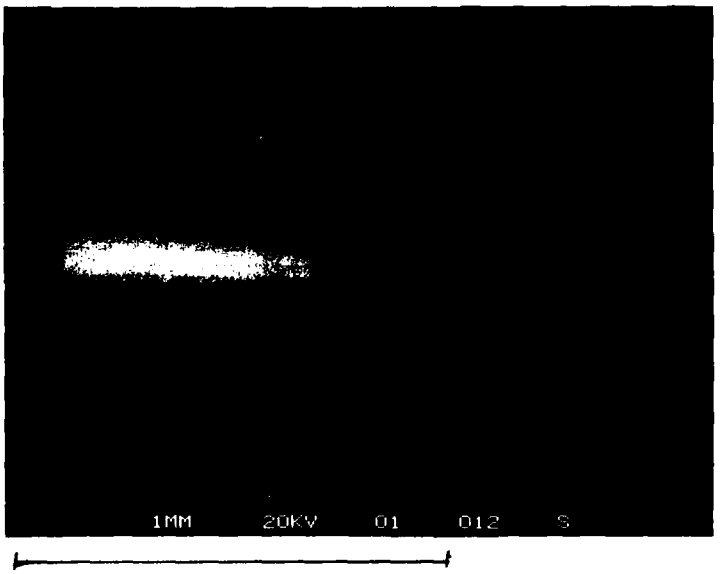


FIG. 51

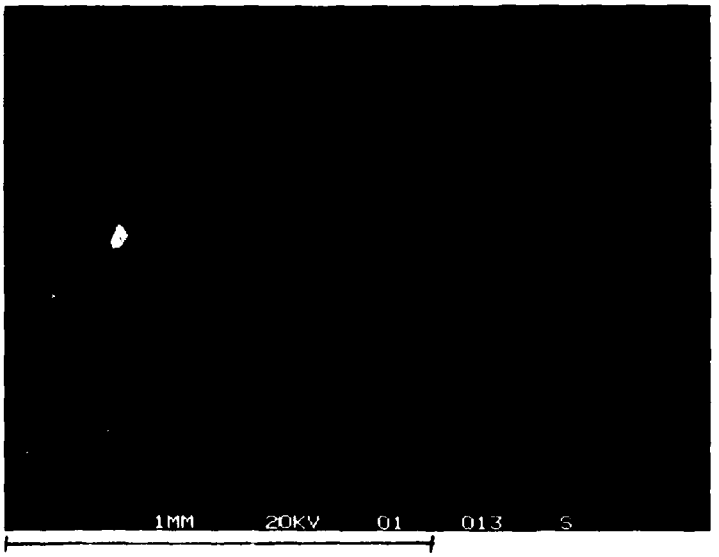


FIG. 52

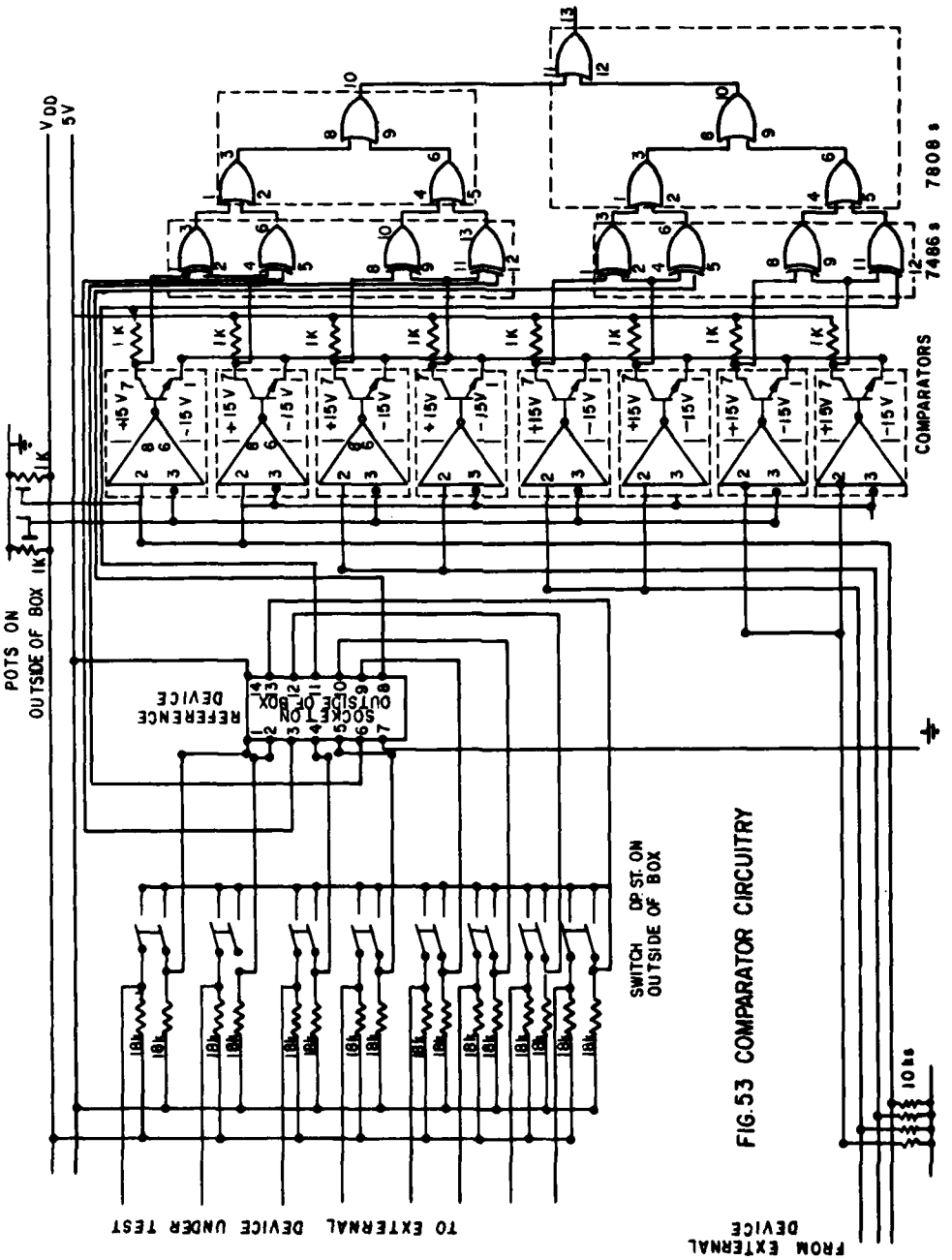


FIG.53 COMPARATOR CIRCUITRY

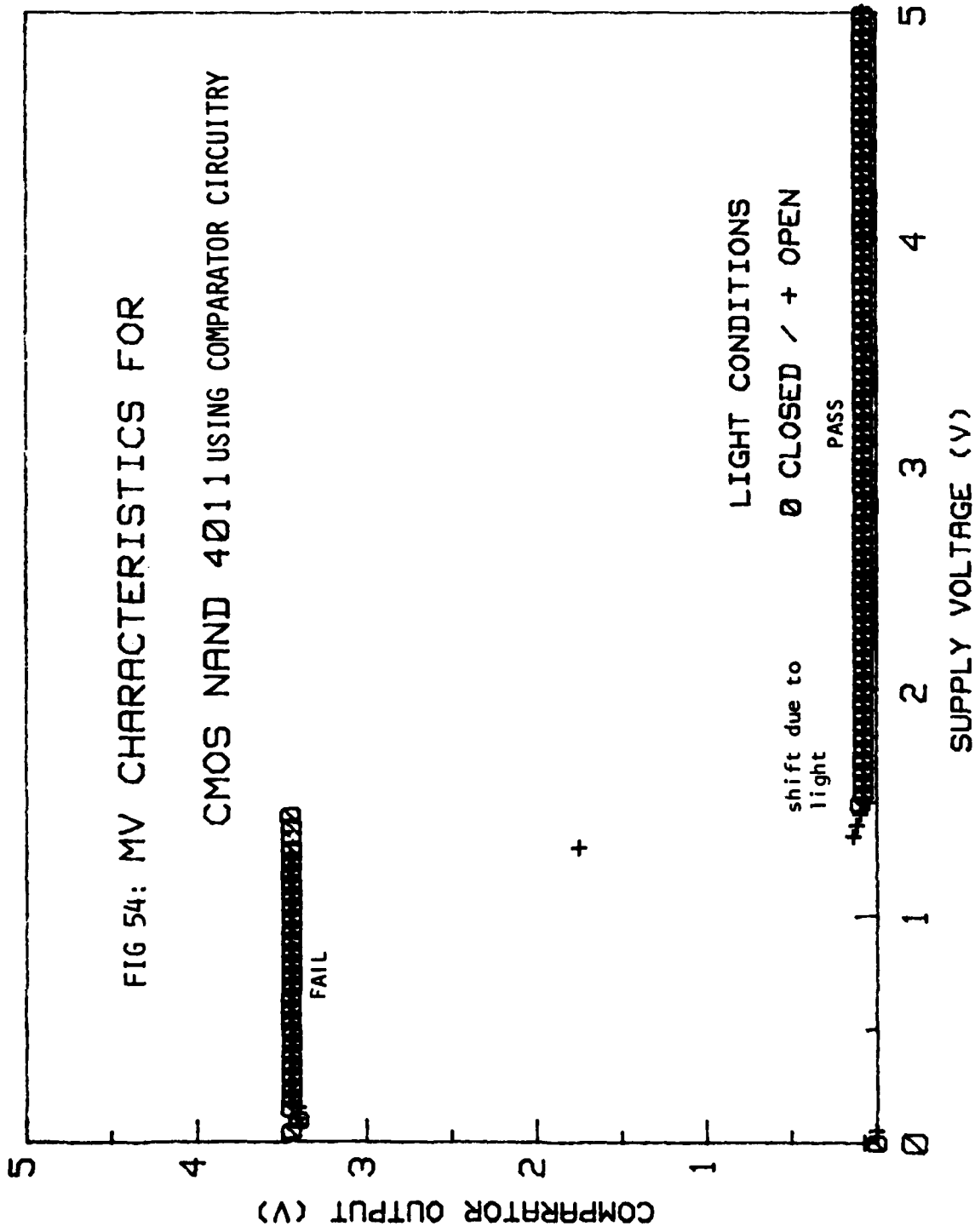


FIG 54: MV CHARACTERISTICS FOR
CMOS NAND 4011 USING COMPARATOR CIRCUITRY
LIGHT CONDITIONS
Ø CLOSED / + OPEN
FAIL
PASS
shift due to light
COMPARATOR OUTPUT (V)
SUPPLY VOLTAGE (V)
0
1
2
3
4
5

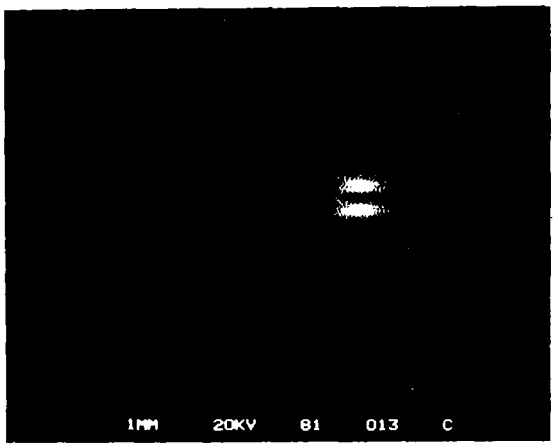


Fig. 55 Gate 1
MV = 1.16V

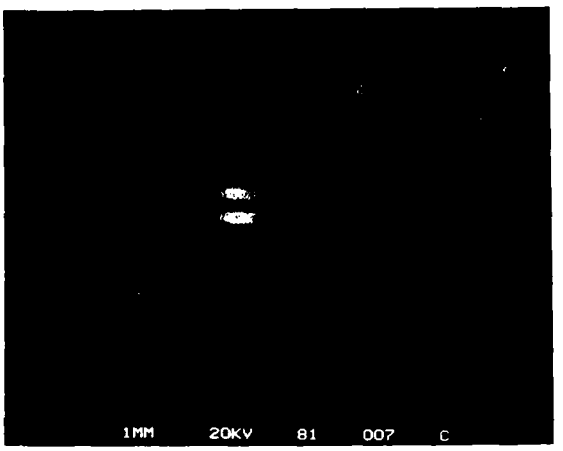


Fig. 56 Gate 2
MV = 1.18V

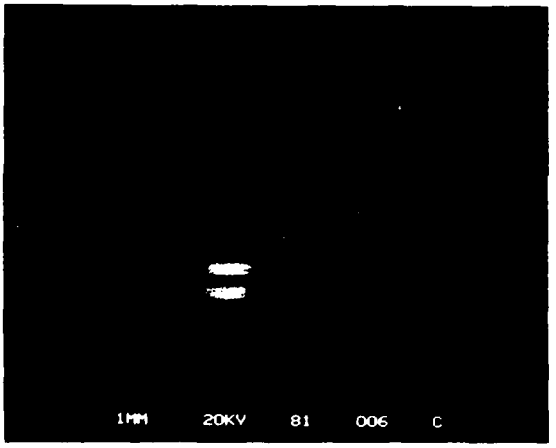


Fig. 57 Gate 3
MV = 1.20V

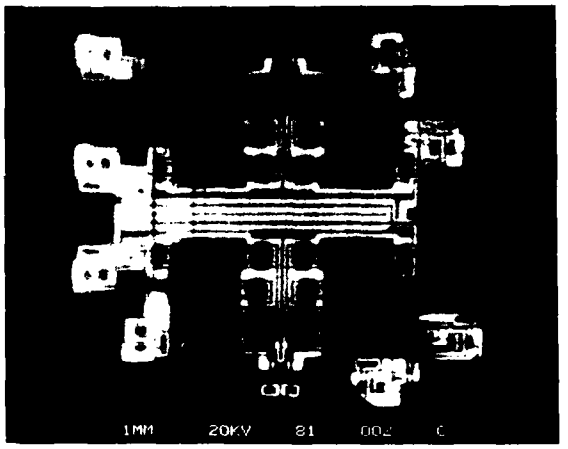


Fig. 58
OBIC IMAGE

Use of SOMSEM and comparator circuitry for imaging different gates under marginal voltage conditions.

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Rome Air Development Center

RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control, Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of competence is provided to ESD Program Offices (POs) and other ESD elements to perform effective acquisition of C^3I systems. The areas of technical competence include communications, command and control, battle management, information processing, surveillance sensors, intelligence data collection and handling, solid state sciences, electromagnetics, and propagation, and electronic, maintainability, and compatibility.

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